AgatePXC, MerlinPXC, and MerlinMTX XMC/PMC Graphics Boards User's Manual

Rastergraf

Rastergraf, Inc.

1810-J SE First St.
Redmond, OR 97756
(541) 923-5530

web: http://www.rastergraf.com

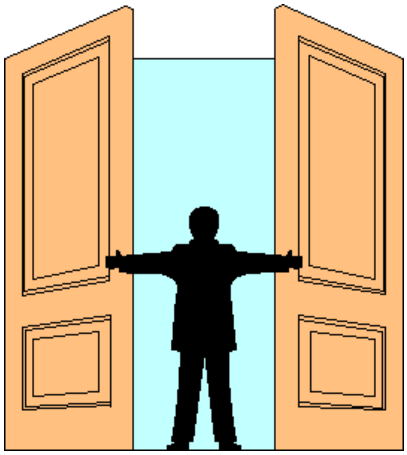
Release 1.3
August 12, 2017

Table of Contents

Tables

Figures

Introduction



This manual provides information about how to configure, install, and program the Rastergraf AgatePXC, MerlinPXC, and MerlinMTX graphics boards.

The AgatePXC uses the AMD E4690 2-display graphics controller with 512MB on-chip GDDR3 memory. The MerlinPXC and MerlinMTX use the AMD E8860 6-display graphics controller with 2GB on-chip GDDR5 memory. While the two boards do use different graphics chips, their designs share many features and thus they are presented in one manual.

The boards are primarily intended for use in XMC and/or PMC-based CPUs. They may also be installed in standard slots of VME, VPX, PCI, or CompactPCI computers when used with a XMC or PMC host adapter.

This manual is broken down into ten chapters:

Chapters 1-3 provide background material. If you want to perform the installation as quickly as possible, start with Chapter 5. If you have problems installing the hardware, refer to Chapter 9 for help.

Getting Help

This installation manual gives specific steps to take to install your Rastergraf board. There are, however, variables specific to your computer configuration and monitor that this manual cannot address. Normally, the default values given in this manual will work. If you have trouble installing or configuring your system, first read Chapter 10, "Troubleshooting".

If this information does not enable you to solve your problems, please contact Rastergraf technical support by sending email to support@rastergraf.com .

If your problem is monitor related, Rastergraf technical support will need detailed information about your monitor.

Board Revisions

This manual applies to the following board revision levels:

AgatePXC Fab Rev 0, 1, 2

MerlinPXC Fab Rev 0

MerlinMTX Fab Rev 0

AgatePXC PIM Fab Rev 0

MerlinPXC PIM Fab Rev 0

MerlinMTX PIM Fab Rev 0

Manual Revisions

Revision 1.0	September 15, 2015	First released version
Revision 1.1	September 10, 2016	Miscellaneous revisions, added MerlinMTX and notes for Agate Rev 0/1.
Revision 1.2	June 10, 2017	Many corrections and improvements
Revision 1.3	August 12, 2017	Minor corrections

Notices

The proprietary information contained in this manual must not be disclosed to others for any purpose without written permission of Rastergraf, Inc. Then use of this manual will be construed as an acceptance of the foregoing condition.

Its sole purpose is to provide the user with adequately detailed documentation to effectively install and operate the equipment supplied. The use of this manual for any other purpose is specifically prohibited

The information provided in this manual, including the specifications of the graphics boards and other components, are subject to change without notice and should not be construed as a commitment by Rastergraf, Inc.

While reasonable precautions have been taken, and although it regrets them, Rastergraf, Inc. assumes no responsibility for any errors or omissions that may occur in this manual. Customers are advised to verify all information contained in this manual.

The electronic equipment described herein generates, uses, and may radiate radio frequency energy, which can cause radio interference. Rastergraf, Inc. assumes no liability for any damages caused by such interference.

Rastergraf, Inc.'s products are **not** authorized for ***any*** use as critical components in flight safety or life support equipment.

These products have been designed to operate in user-provided XMC or PMC-compatible computers. Connection of incompatible hardware is likely to cause serious damage. Rastergraf, Inc. assumes no liability for any damages caused by such incompatibility.

Rastergraf assumes no responsibility for the use or reliability of software or hardware that is not supplied by Rastergraf, Inc., or which has not been installed in accordance with this manual.

Rastergraf is a trademark of Rastergraf, Inc.

All brand and product names are trademarks or registered trademarks of their respective owners.

Copyright © 2017 by Rastergraf, Inc.

Conventions Used In This Manual

The following list summarizes the conventions used throughout this manual.

`Code fragments`	Code fragments, file, directory or path names and user/computer dialogs in the manual are presented in the `courier` typeface.
Commands or **program names**	Commands, or the names of executable programs, except those in code fragments, are in bold.
System prompts and commands	Commands in code fragments are preceded by the system prompt, a percentage sign (%), the standard prompt in UNIX's C shell, or the hash mark (#), the standard UNIX prompt for the Super-User.
Keyboard usage	**<CR>** stands for the key on your keyboard labeled "RETURN" or "ENTER"

Note	Note boxes contain information either specific to one or more platforms, or interesting, background information that is not essential to the installation.

Caution	Caution boxes warn you about actions that can cause damage to your computer or its software.

Warning!	Warning! boxes warn you about actions that can cause bodily or emotional harm.

Signal Conventions

The following table lists symbols that can follow a signal name. For example, the asterisk (*) is used with a VMEbus signal name, such as BERR*.

Symbol	Description
_n or * or L or #	The signal is active LOW.
H or [no symbol]	The signal is active HIGH.

Memory Sizes and Addresses

The following table lists the abbreviations used to describe the size of a memory device or a range of addresses.

Abbreviation	Convention
1 Kbit or 1 Kb	1,024 bits
1 Kbyte or 1 KB	1,024 bytes
1 Mbit or 1 Mb	1,024 Kbits
1 Kbyte or 1 KB	1,024 bytes
1 Gbyte or 1 GB	1,024 Mbytes

Related Documents

This manual is the self-contained documentation for the AgatePXC, MerlinPXC, and MerlinMTX.

The boards can be installed in a wide variety of systems which would use an x86 or PowerPC CPU. It is beyond this the scope of this manual to cover the installation of these system components or their system software.

Suffice it to say that you should consult the relevant software documentation and the manual for the Single Board Computer on which your Rastergraf graphics board is installed. Please note that is it ***always*** a good idea to make sure that your basic system is operating correctly before installing board options such as a graphics board.

In the event of any uncertainty, please contact Rastergraf at support@rastergraf.com.

Chapter 1
General Information

1.1 Introduction

The AgatePXC, MerlinPXC, and MerlinMTX graphics boards are closely related designs that have been tuned to address a variety of requirements. The boards are intended for use in XMC and/or PMC-based CPUs but may also be installed in any VME, VPX, PCI, or CompactPCI computer when used with a suitable host adapter. Regrettably, AMD doesn't support the E4690 used on the AgatePXC beyond Windows 7.

The graphics boards are ideal for air-cooled benign and moderately harsh environments that are found in both commercial and military applications. They are available in Levels 0, 50, and 100 of air-cooled configurations and can be supplied with a conformal coating.

While compliant with the Conduction-Cooled PMC form factor (except at the front panel connectors), the AgatePXC and MerlinPXC are not intended for use in conduction-cooled systems.

However, the MerlinMTX can indeed be used in conduction-cooled (Level 100) environments and follows the VITA 20 CCPMC mounting and form-factor specifications. As such, it is not delivered with a heat sink or front panel. Rastergraf has worked with a third party (Mistral Solutions) to provide a complete conduction-cooled solution. Please contact Rastergraf for more information.

The following pages provide Functional Descriptions and block diagrams of each board followed by a comparative table of features.

Section 1.1.1 AgatePXC Functional Description and block diagrams

Section 1.1.2 MerlinPXC Functional Description and block diagrams

Section 1.1.3 MerlinMTX Functional Description and block diagrams

Table 1-1 Feature Comparison

Sections 1.2 and on cover each board's major components.

PMC Users – Please Read This

Please note that while the Agate and Merlin are designed to work (and indeed DO work) in both PMC and XMC systems, very high speed controllers are used in the designs for video acquisition: CX25858 (Agate and MerlinMTX), CX3 and FX3 for Agate, and CX3 for the MerlinPXC.

If you plan to run on a PMC host and use the acquisition subsystems, you **must have** at least 32-bit 66 MHz PCI. Even so, we have seen cases where some systems just freeze. In general PCIe is much preferred.

If your system doesn't support 64-bit PCI and/or 100 or 133 MHz, there is no alternative but to use XMC.

Figure 1-1 AgatePXC Side 1

Figure 1-2 AgatePXC Side 1 with Heat Sink Installed

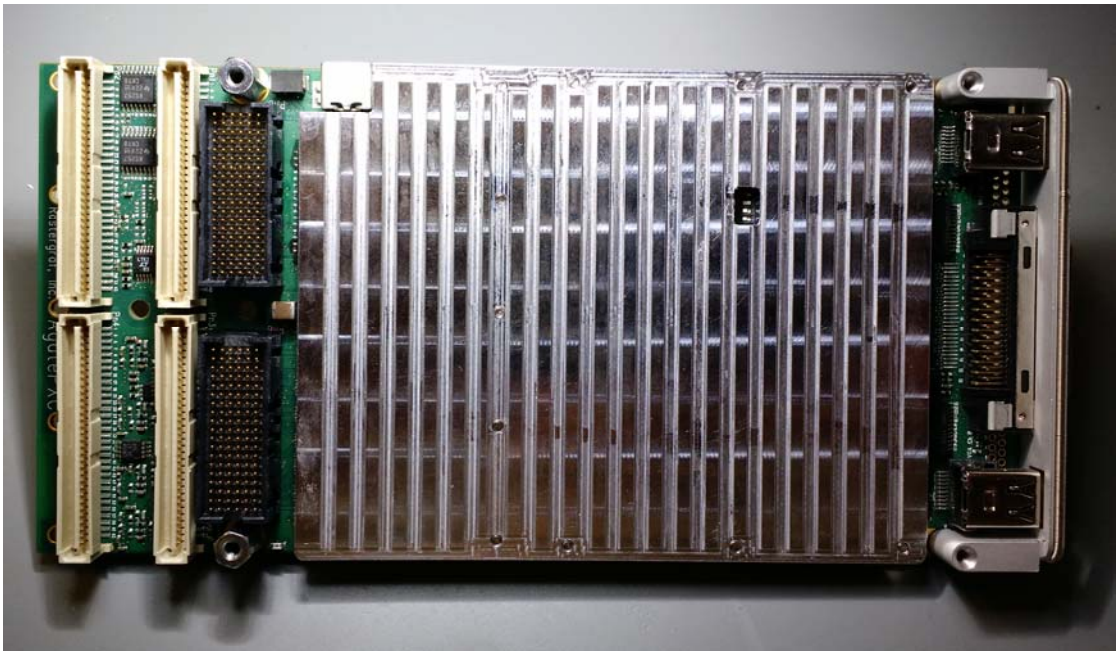


Figure 1-3 AgatePXC Side 2

1.1.1 AgatePXC Functional Description

Note that the AMD accelerated display driver does not work beyond Windows 7 so the Agate is not recommended for Windows 8 – 10.

The AgatePXC is designed to satisfy requirements for a complete graphics and video acquisition solution. It automatically detects a XMC or PMC host. In a dual-bus footprint, it defaults to XMC.

An IDT 24T6G2 PCIe 2.0 switch arbitrates between local PCIe devices and the XMC x8 port. For PMC, a Pericom 9X130 PCIe/PCI bridge supports PMC host interfaces from 32-bit, 33 MHz PCI to 64-bit, 133 MHz PCI-X via a PCIe 1.0 x4 link.

The AgatePXC uses the AMD Radeon E4690 Graphics Processor, which includes 320 shader processors, a 128-bit memory interface, and 512MB of GDDR3 on-chip memory. The E4690 provides hardware support for OpenGL 3.0 and DirectX 10.1 as well as H.264, VC-1, and MPEG-2 video codecs. Multiple HD video streams can be decoded at once.

Screen resolutions up to 2560x1600 are available using the AgatePXC/2 standard dual DisplayPort 1.1a outputs that are provided on front panel Mini DisplayPort (mDP) connectors. External “dongles” can transparently convert the mDP to DVI, VGA, NTSC/PAL, and full-size DP connector.

As configured in the standard AgatePXC/2 version, a front panel SDR50 I/O connector provides links to:

1) a Conexant CX25858 audio/video digitizer that can at once capture two stereo audio and eight NTSC/PAL video streams,
2) a single E4690 video output with VGA, YPrPb, STANAG 3350 A/B/C, composite, and S-Video modes,
3) an Analog Devices ADV7441A digitizer that can capture RGBHV at up to 1600x1200 via a Cypress FX3 USB 3.0 controller,
4) a MIPI CSI-2 camera port via a Cypress CX3 USB 3.0 controller.

Display-only versions provide dual VGA, dual mini DisplayPort (mDP), or a single LVDS single or dual link port.

A VITA 36 PMC I/O Module (PIM) with MIPI and YUV camera adapter boardlets are also available to ease connectivity to the Agate.

The Integrated System Monitor (ISM) uses an ST Micro STM32F427 32-bit CPU to provide Built-In Self Test (BIST) and real-time monitoring of most board functions using I^2C /SMbus, JTAG, voltage, and temperature. Reporting is done via LEDs and USB.

Although not a conduction-cooled design, the AgatePXC is laid out in a Conduction Cooled PMC (CCPMC) compatible format with Primary and Secondary Thermal Interface area for easy use in all environments.

Figure 1-4 AgatePXC Block Diagram

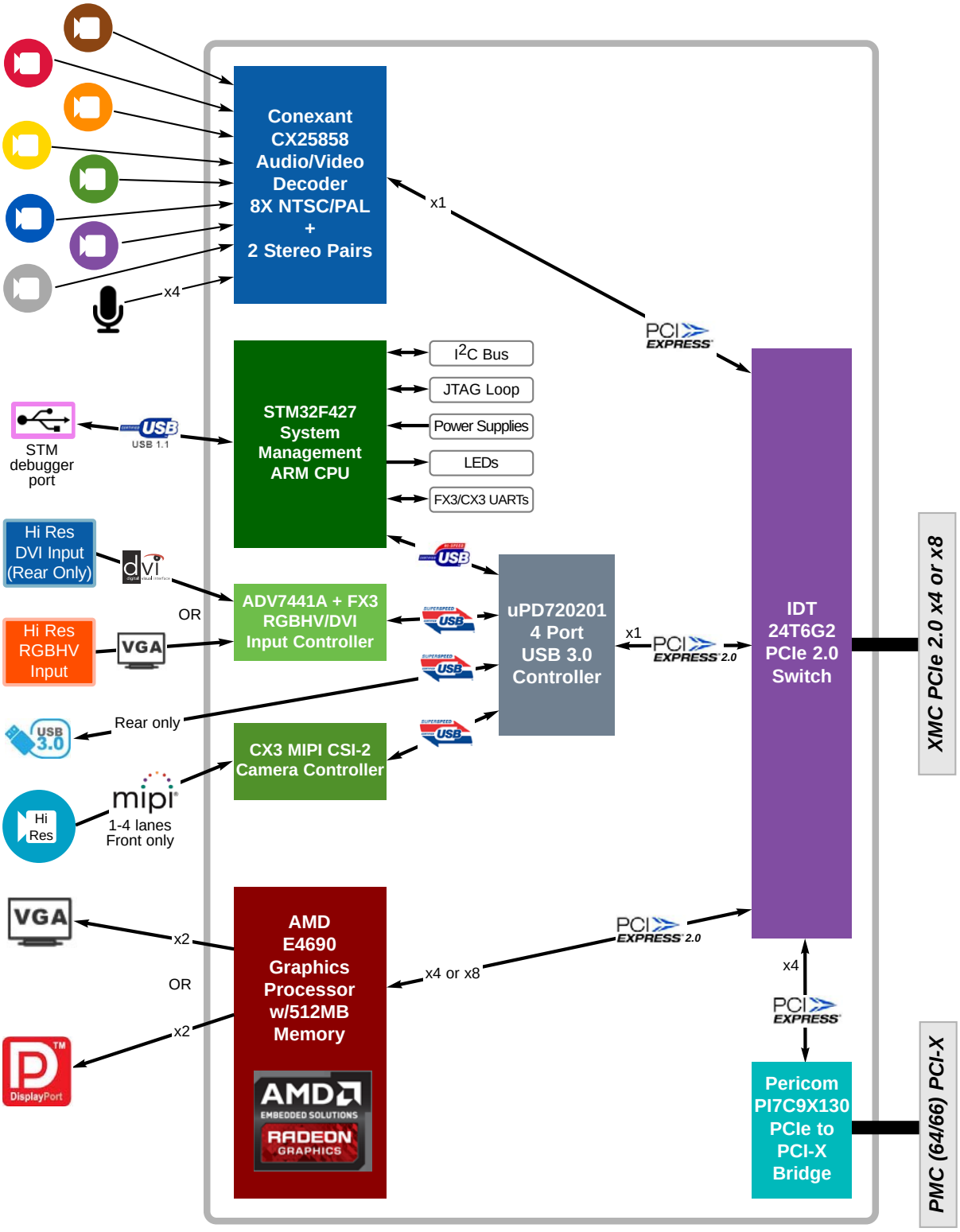


Figure 1-5 AgatePXC Comprehensive Block Diagram

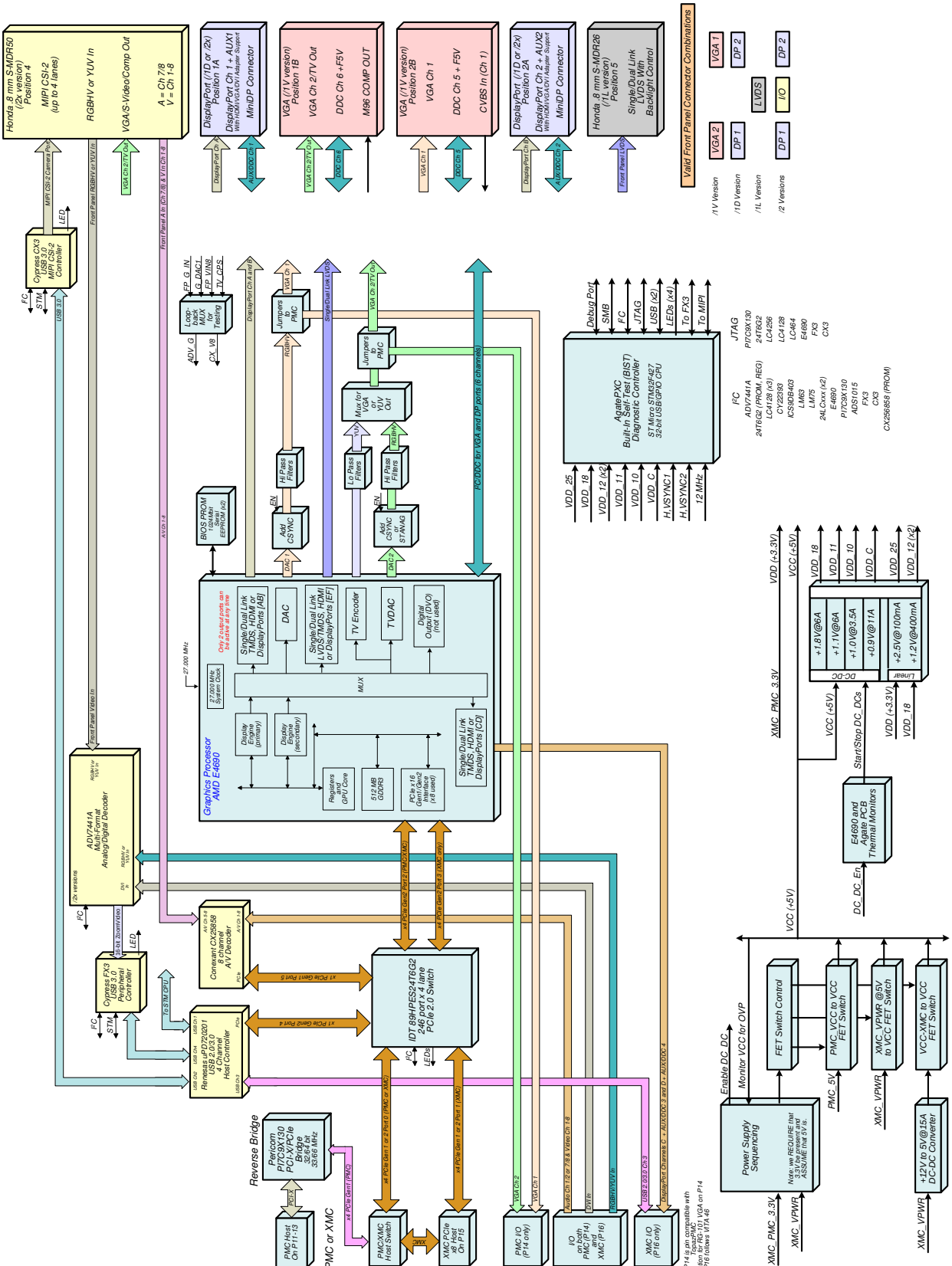


Figure 1-6 AgatePXC Parts Locations

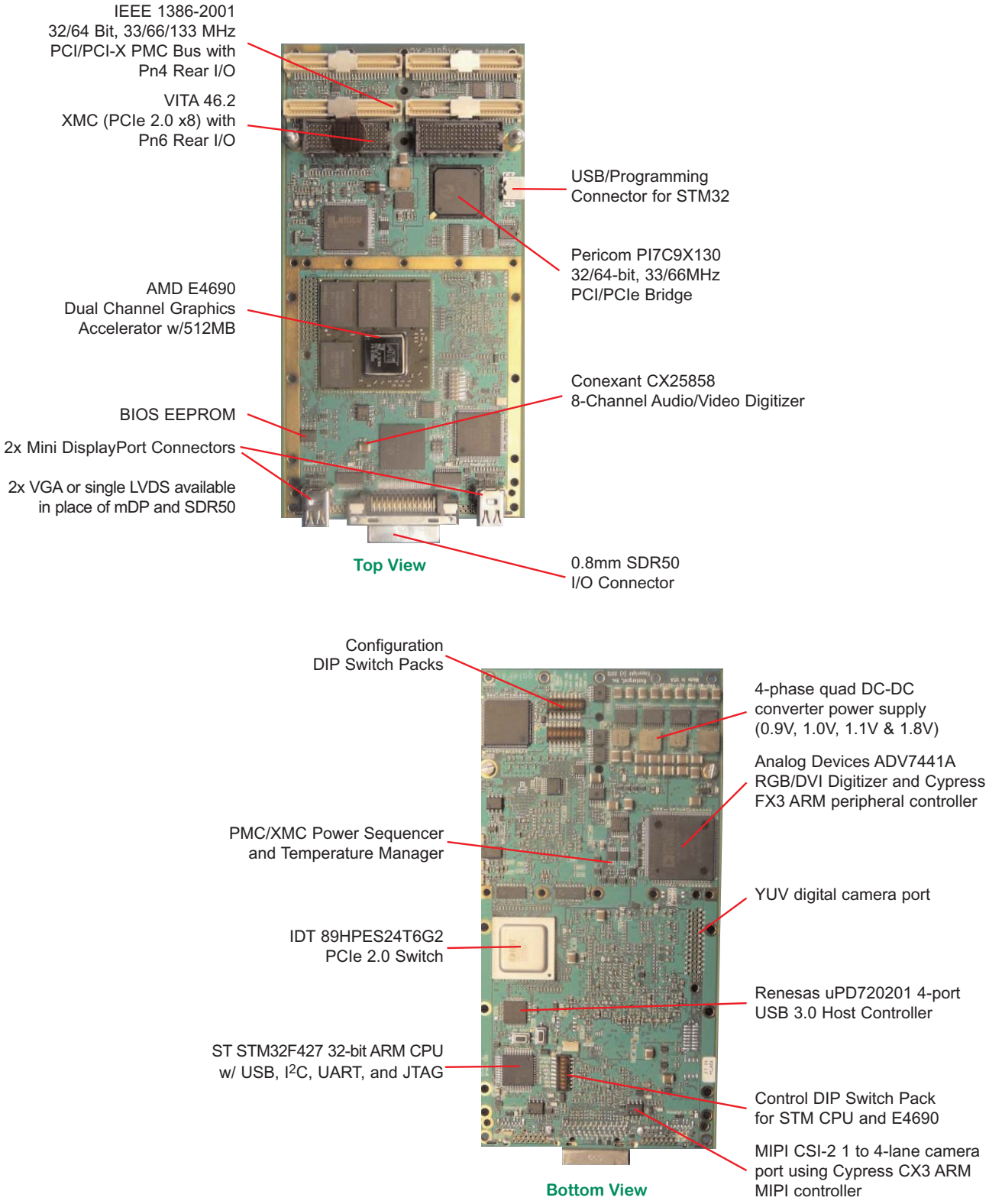


Figure 1-7 AgatePXC PIM Block Diagram

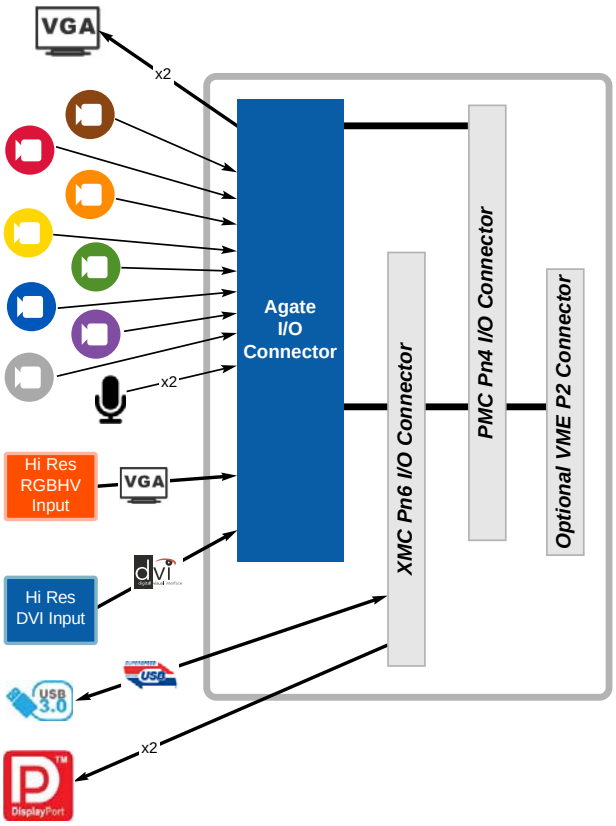


Figure 1-8 AgatePXC PIM Parts Locations

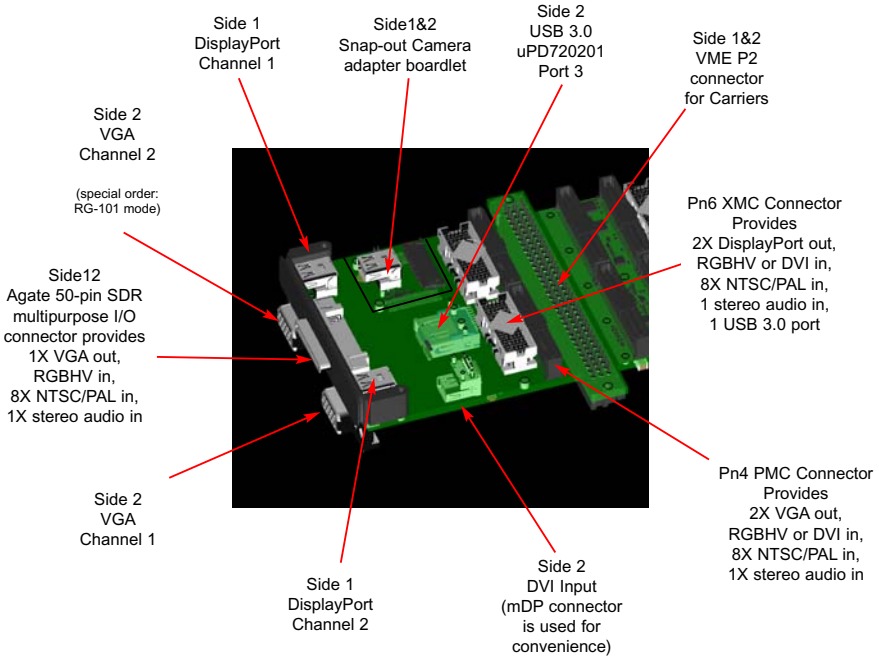


Figure 1-9 MerlinPXC Side 1

Figure 1-10 MerlinPXC Side 2

1.1.2 MerlinPXC Functional Description

The MerlinPXC design is derived from the older AgatePXC (AMD dropped support beyond Windows 7). The Merlin uses the AMD E8860, which is 2 generations beyond the Agate's E4690. The Merlin's focus is on supporting multiple displays, and making connections both front and rear it can support 6 displays at one time.

Like the Agate, it can be used in an XMC, PMC, or XMC/PMC footprint and can operate in XMC locations with VPWR set to 5V or 12V. In a dual-bus footprint, it defaults to XMC.

An IDT 24T6G2 PCIe 2.0 switch arbitrates between on-board PCIe devices and the XMC x8 port. For PMC, a Pericom 9X130 PCIe/PCI bridge supports PMC host interfaces from 32-bit, 33 MHz PCI to 64-bit, 133 MHz PCI-X via a PCIe 1.0 x4 link.

The MerlinPXC uses the AMD Radeon E8860 Graphics Processor, which includes 640 shader processors, a 128-bit memory interface, and 2MB of GDDR5 on-chip memory. Extensive standards support includes OpenGL 4.2, Open CL 1.2, DirectX 11.1, dual-stream HD as well as H.264, VC-1, and MPEG-2 HD and MPEG-4 DivX and Xvid.

Screen resolutions up to 4096 × 2160 @ 30 Hz can be had through each of the Merlin's 6 DisplayPort 1.1a/2.0 outputs. Multiple screens can be supported on each output by way of DP 1.2's higher link speeds and multi-stream transport function.

Four Mini DisplayPort (mDP) connectors are provided on the front panel and 3 outputs (one shared with the front) are available on the rear access XMC Pn6 and PMC Pn4 connectors. Low-cost external in-line "dongles" can transparently convert the mDP to DVI, VGA, NTSC/PAL, or LVDS.

High resolution video can be captured via the front panel MIPI CSI-2 port using a Cypress CX3-based processor linked to one of the Merlin's USB 3.0 ports.

Display-only versions (no MIPI) include the single VGA MerlinPXC/1V and the 4 front panel Mini DisplayPort MerlinPXC/1D.

A VITA 36 PMC I/O Module (PIM) with a MIPI camera adapter boardlet are also available to ease connectivity to the Merlin.

The Integrated System Monitor (ISM) uses an ST Micro STM32F427 32-bit CPU to provide Built-In Self Test (BIST) and real-time monitoring of most board functions using I^2C /SMbus, JTAG, voltage, and temperature. Reporting is done via LEDs and USB.

Although not a conduction-cooled design, the MerlinPXC is laid out in a Conduction Cooled PMC (CCPMC) compatible format with Primary and Secondary Thermal Interface area for easy use in all environments.

Figure 1-11 MerlinPXC Block Diagram

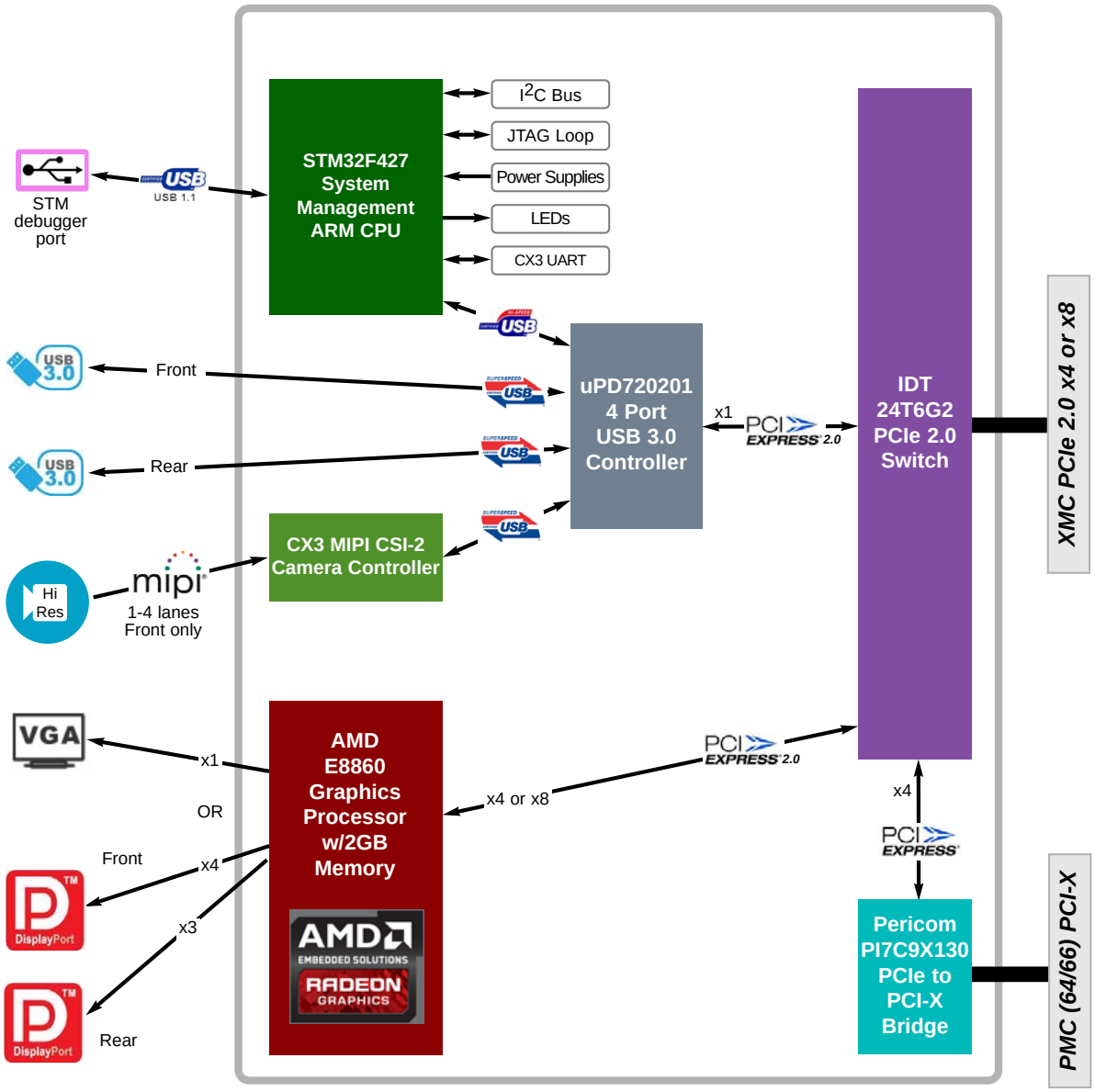


Figure 1-12 MerlinPXC Comprehensive Block Diagram

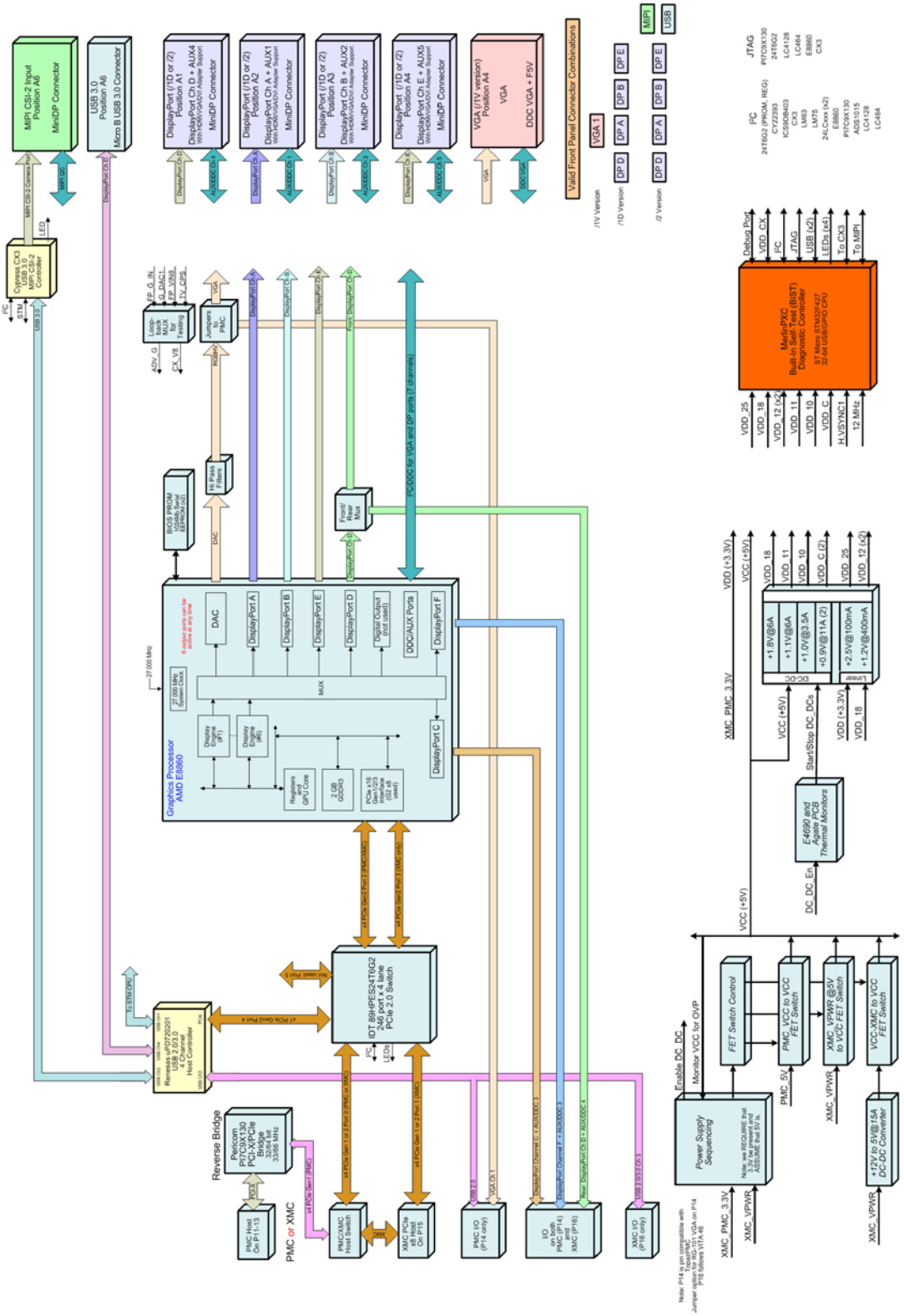
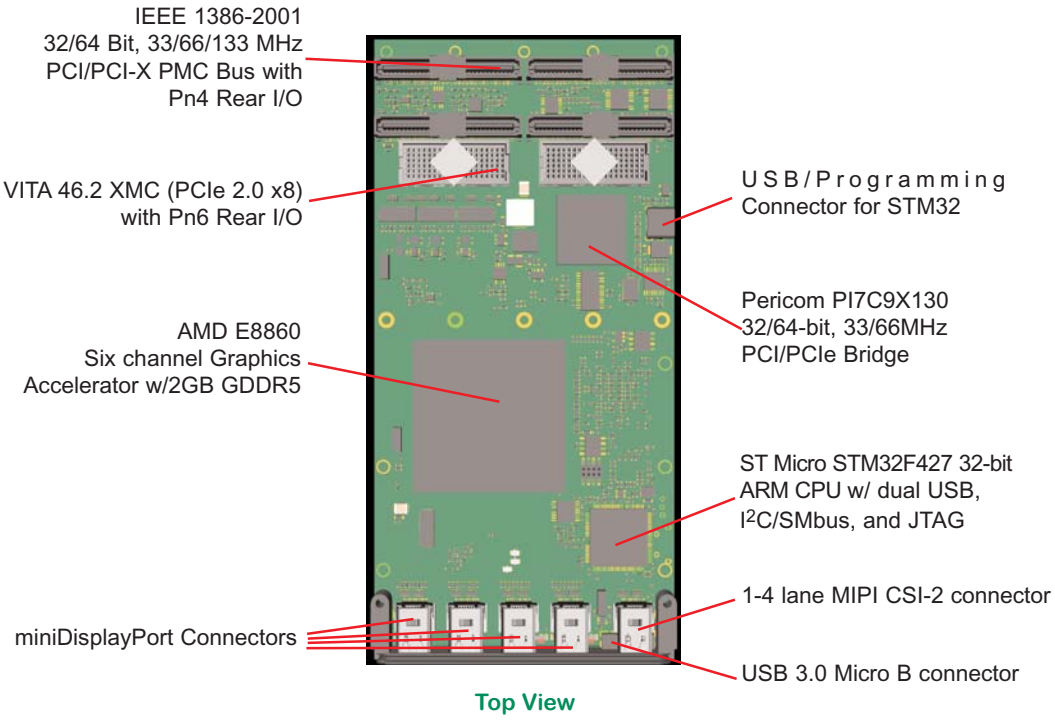
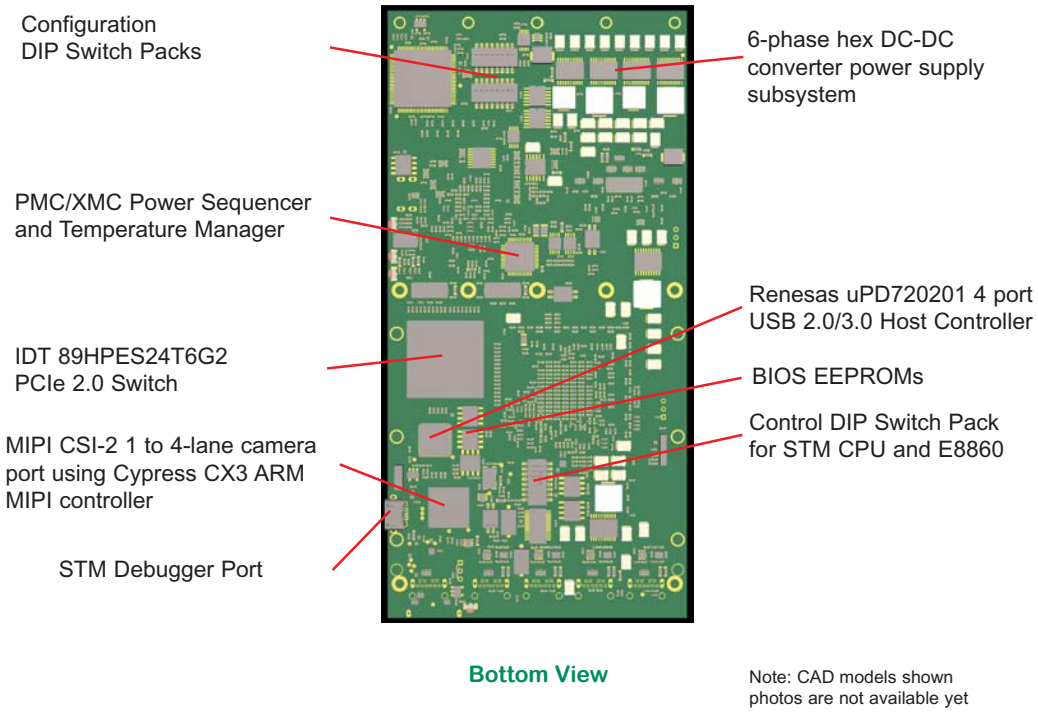


Figure 1-13 MerlinPXC Parts Locations





Note: CAD models shown photos are not available yet

Figure 1-14 MerlinPXC PIM Block Diagram

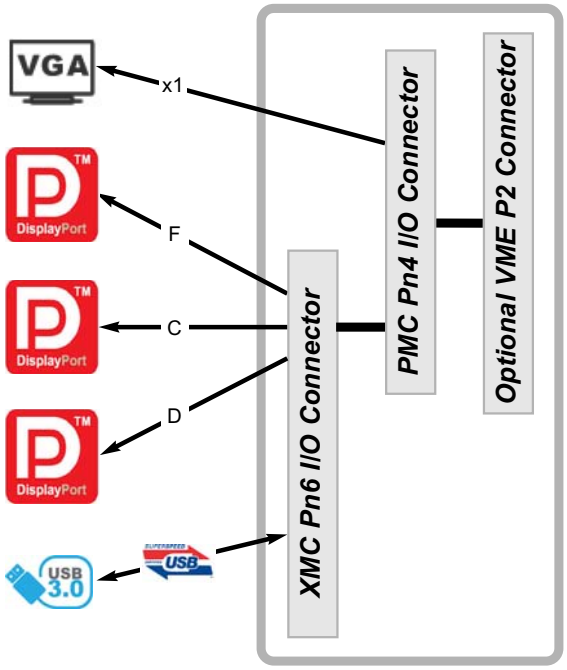


Figure 1-15 MerlinPXC PIM Parts Locations

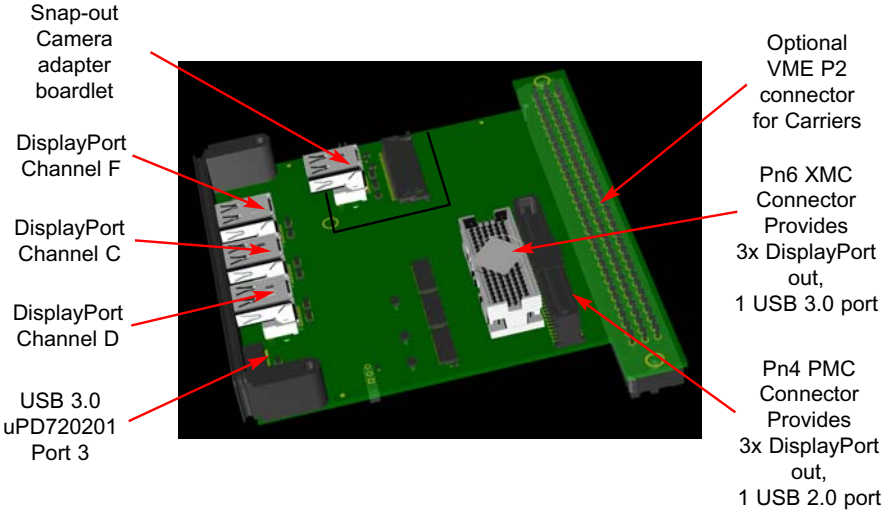
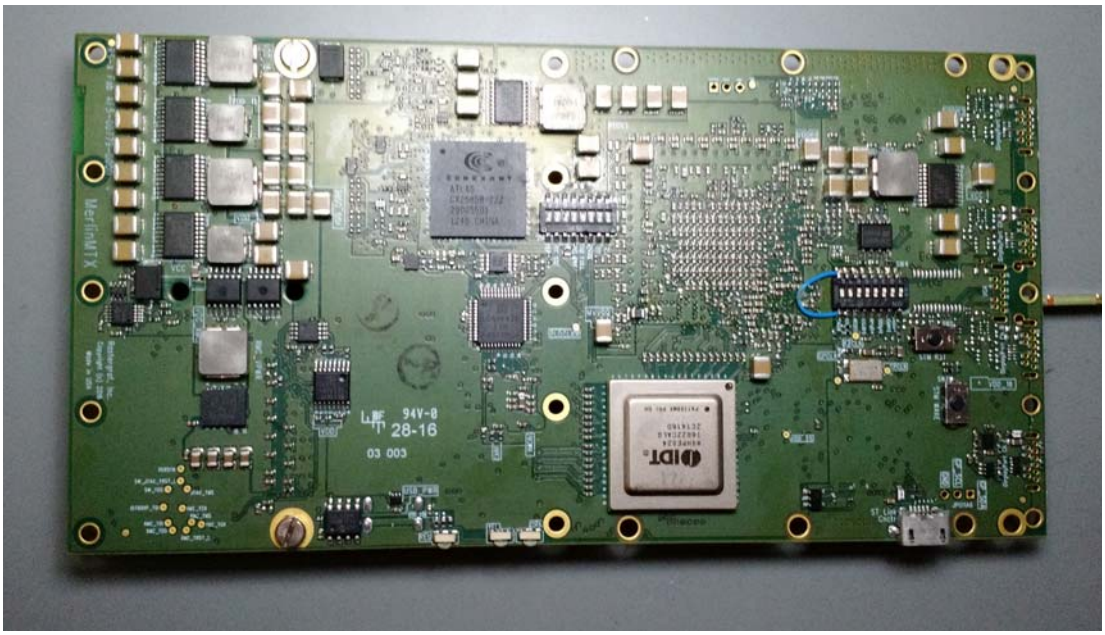


Figure 1-16 MerlinMTX Side 1

Figure 1-17 MerlinMTX Side 2



1.1.3 MerlinMTX Functional Description

The MerlinMTX is a special purpose design derived from the MerlinPXC and thus has many features in common with it. The MerlinMTX's focus is on providing video input and DVI outputs on PMC (Pn4) and supporting conduction-cooled applications.

Unlike the AgatePXC or MerlinPXC, the MerlinMTX works ONLY in an XMC Pn5 host position (with VPWR set to 5V or 12V) and provides rear I/O ONLY on the PMC Pn4 connector.

Other deletions include the USB and MIPI controllers, XMC Pn6 I/O, and PMC bus access.

On the plus side, a Conexant CX25858 audio/video digitizer has been added that can capture several NTSC or PAL video streams at one time.

A VITA 36 PMC I/O Module (PIM) mapped to PMC Pn4 is available that breaks out the 2 DVI ports or, alternately, the single DisplayPort output. DVI Channel F uses a DVI-I connector. It maps the DVI-I connector's RGBH VGA pins to the CX25858 video inputs.

As a VITA 20 CCPMC-compliant board, the standard MerlinPXC does not provide any front panel connections nor even the front panel itself, as a CCPMC installation does not provide room for one.

Please note that it is not Rastergraf's intention to serve the general ruggedized, conduction-cooled market. The MerlinMTX is special board only suited to particular applications within that market and is available only to highly-qualified customers.

Please contact Rastergraf at sales@rastergraf.com if you feel that you have an application that would call for the MerlinMTX.

Figure 1-18 MerlinMTX Block Diagram

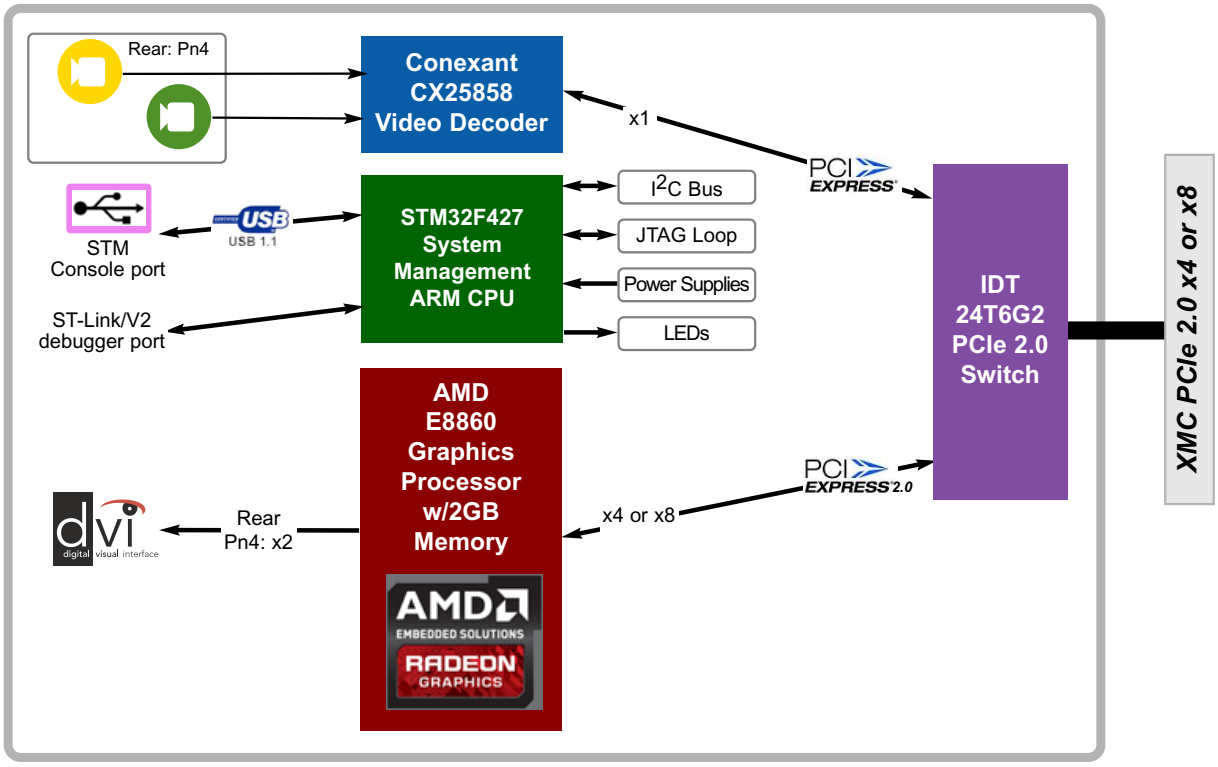


Figure 1-19 MerlinMTX Comprehensive Block Diagram

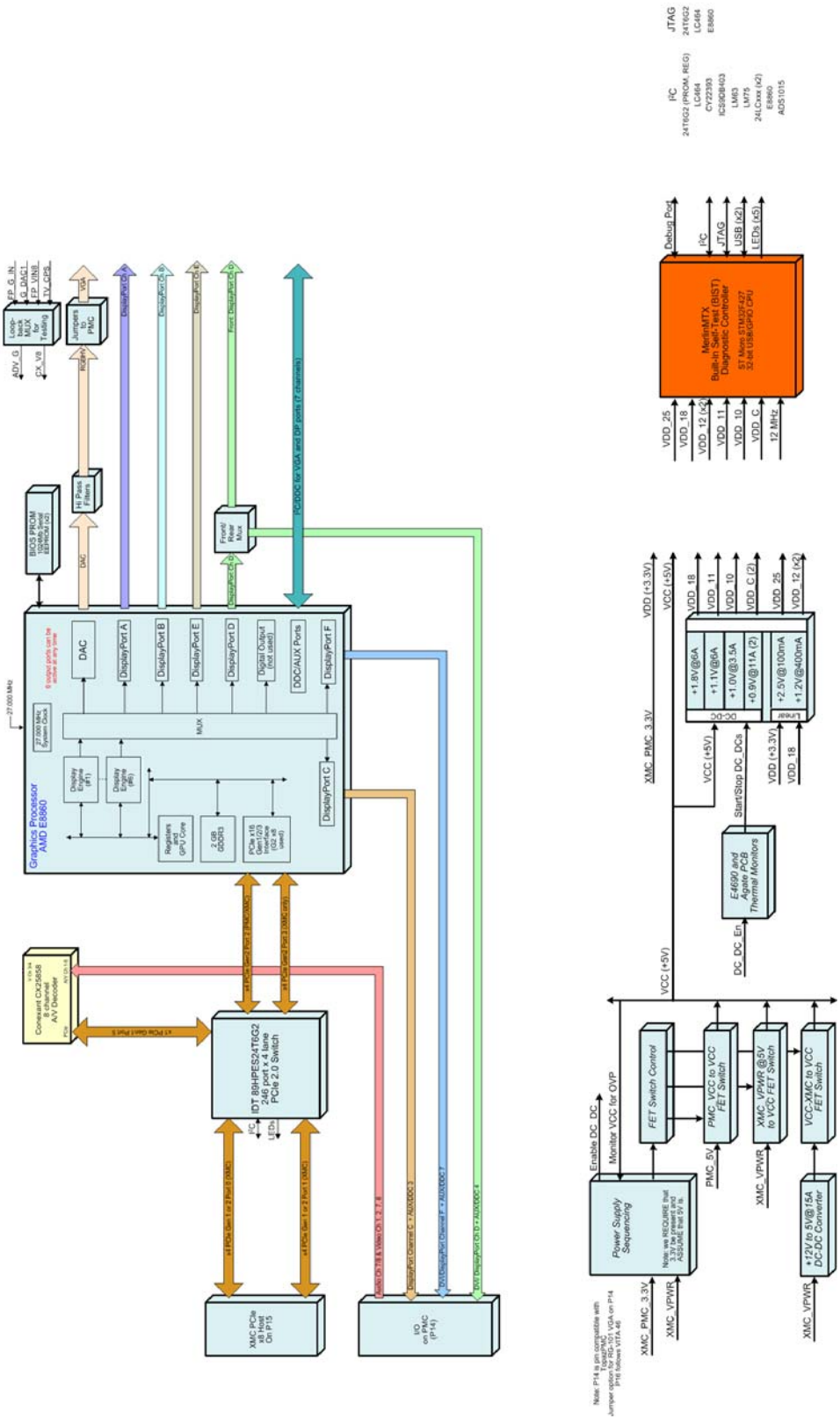
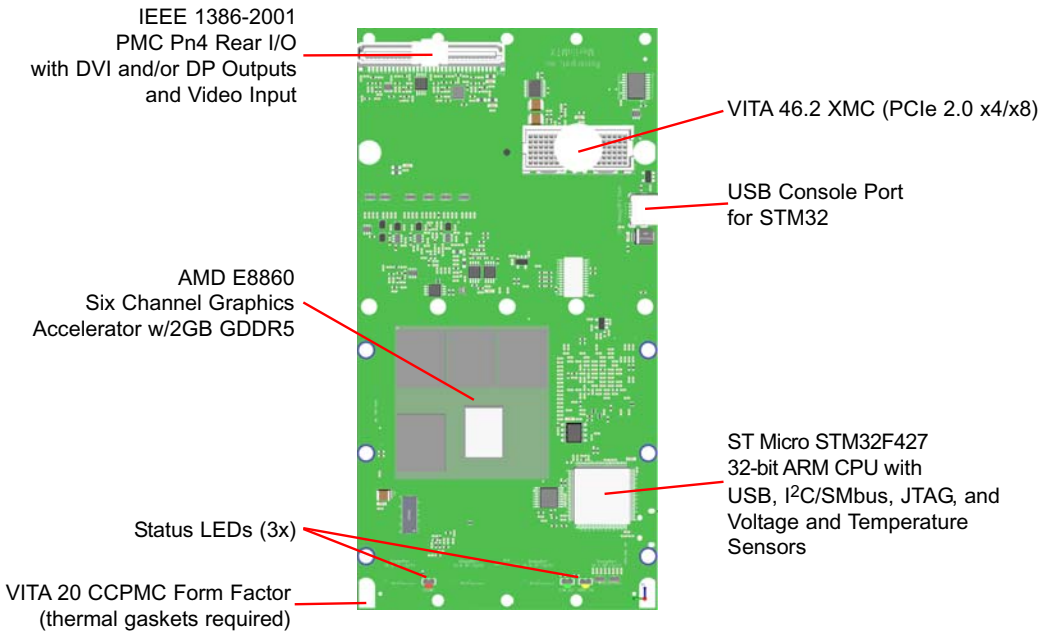
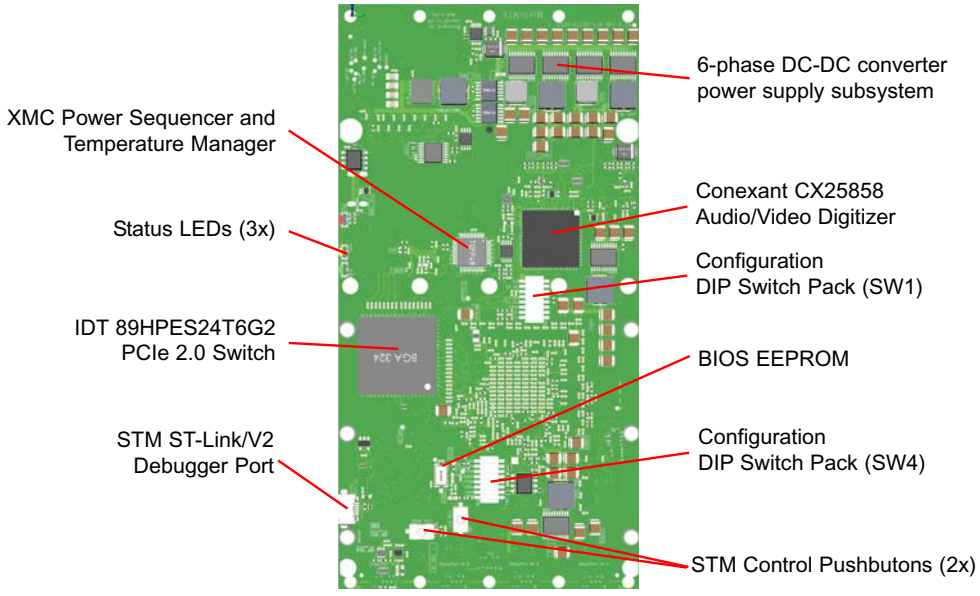


Figure 1-20 MerlinMTX Parts Locations



Top View



Bottom View

Note: CAD models shown
photos are not available yet

Figure 1-21 MerlinMTX PIM Block Diagram

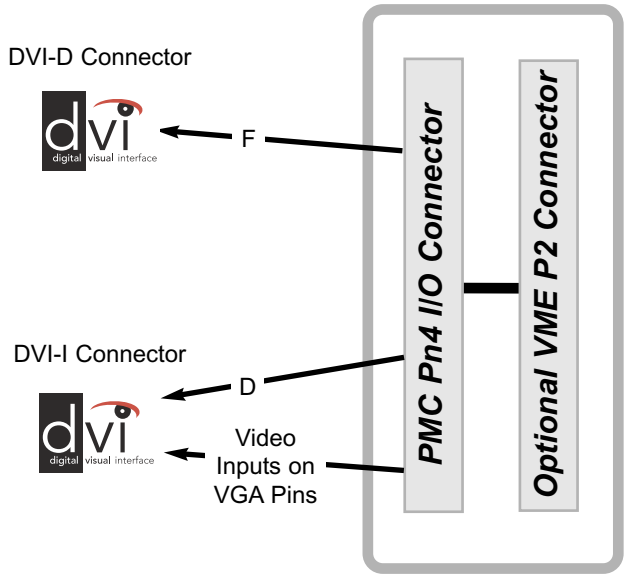


Figure 1-22 MerlinMTX PIM Parts Locations

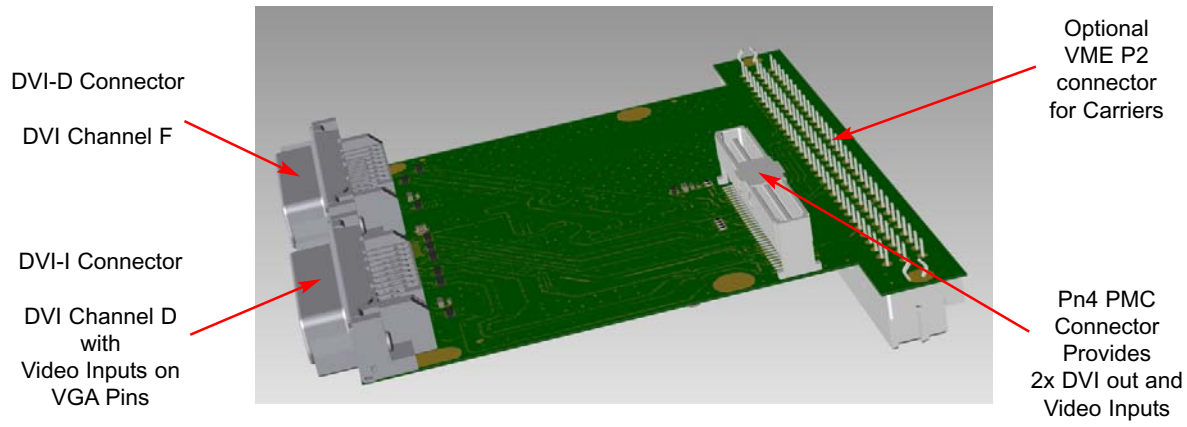
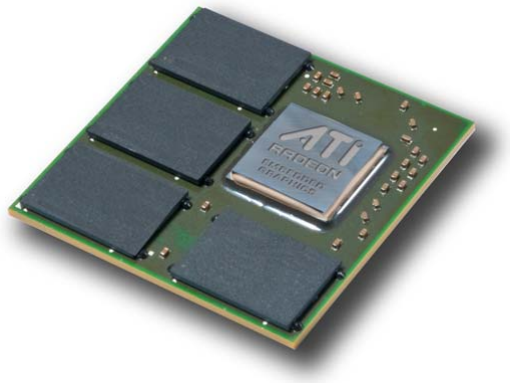


Table 1-1 Feature Comparison

	AgatePXC	MerlinPXC	MerlinMTX
AMD E4690, 2 display channels, 512MB GDDR3	**yes**		
AMD E8860, 6 display channels, 2GB GDDR5		**yes**	**yes**
Front Panel DisplayPort Outputs	**2**	**4**	
PMC/XMC Bus Support	**PMC/XMC**	**PMC/XMC**	**XMC Pn5**
PMC/XMC Rear Panel I/O	**PMC/XMC**	**PMC/XMC**	**PMC Pn4**
Rear Panel DisplayPort Outputs	**2**	**3**	**1 (optional)**
DVI outputs (PMC Pn4 only)			**2**
VGA output	**2 (optional)**	**1 (optional)**	
Single LVDS output	**optional**		
Single S-Video/NTSC/PAL output	**yes**		
RGBHV/DVI Input with Cypress FX3 controller	**yes**		
Multi-channel NTSC/PAL Input with Stereo Audio In	**yes**		**yes**
MIPI CSI-2 1-4 Lane Camera Input w/Cypress CX3 controller	**yes**	**yes**	
4-channel USB 3.0 Controller	**yes**	**yes**	
STM32F327 BIST Controller with USB access and ISM	**yes**	**yes**	**yes**
Thermal and Voltage sensing	**yes**	**yes**	**yes**
JTAG/ I^2C /SMB diagnostics	**yes**	**yes**	**yes**
Debugger port access to STM32F327	**yes**	**yes**	**yes**
Status LEDs	**yes**	**yes**	**yes**
256Kb local configuration serial EEPROM	**yes**	**yes**	**yes**
3.3V & 5V PCI Bus Signaling	**yes**	**yes**	
PCI/PCI-X 33/66/100/133 MHz PCI Bus Speed	**yes**	**yes**	
XMC PCIe 2.0 with up to 8x port width	**yes**	**yes**	**yes**
Vital Product Data (VPD) support for XMC	**yes**	**yes**	**yes**
Field reprogrammable BIOS	**yes**	**yes**	**yes**
Four thermal sensors monitor GPU and board temperatures	**yes**	**yes**	**yes**
PIM Rear I/O adapter	**yes**	**yes**	yes
RG-101-compatible VGA Rear configuration	**optional**	**optional**	
Multi-phase DC-DC supply for reduced noise	**yes**	**yes**	**yes**
SDL Graphics Subroutine Package for Linux and VxWorks	**limited**		
Windows graphics drivers	**XP/W7 only**	**XP-W10 ***	**XP-W10 ***
Linux graphics drivers	**yes**	**yes**	**yes**
VxWorks OpenGL driver	**3rd Party**	**3rd Party**	**3rd Party**
Windows video input drivers	**yes**	**yes**	**yes**
Available with conformal coating and extended temperature	**yes**	**yes**	**yes**
CCPMC form factor compatible	**yes**	**yes**	**yes**
Conduction-cooled version available			**yes**

* Rastergraf recommends W10-64 Pro. XP – W8 versions are no longer adequately protected from new bugs and hacks. That said, E8860 drivers are available for as far back as XP. Please contact Rastergraf for more information

1.2 E4690 Graphics Controller (AgatePXC)



1.2.1 Overview

The AMD Radeon E4690 embedded Graphics Processing Unit (GPU) makes use of a Unified Superscalar Shader architecture, and is fabricated on 55 nm manufacturing process. The chip's maximum graphics engine frequency is 600 MHz. It has 8 color ROPs along with 32 texture units.

The 320 stream processors produce up to 3.88 GFLOPS of peak single-precision performance. The stream processing power is accessed through the ATI Stream SDK, including the compiler, device driver, performance libraries, and performance profiling tools.

The E4690 GPU includes support for DirectX 10.1 and OpenGL 3.0. The second-generation AMD Unified Video Decoder (UVD 2.0) includes hardware acceleration of H.264 and VC-1 high-definition (HD) video as well as MPEG-2, enabling multiple HD video streams to be decoded simultaneously, delivering features like picture-in-picture and freeing the CPU for other tasks.

The E4690 incorporates 512 MB of 700 MHz GDDR3 graphics memory on chip and utilizes 128 bit bus, providing an effective memory bandwidth of 22.4 GB/s.

Incorporating AMD PowerPlay intelligent power management technology, the E4690 optimizes power consumption with exceptional scalability of performance between 8W and 25W.

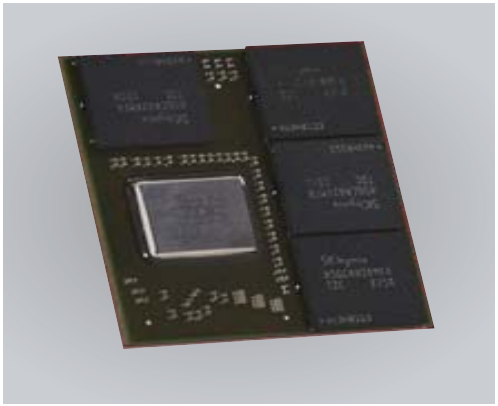
Two independent display controllers each support a resolution of up to 2048 x 1536 pixels. Output options include integrated DisplayPort, single & dual-link LVDS, and dual analog outputs.

The GPU supports PCI Express 2.0 interface. The E4690 is packaged as a 35mm square Multi-Chip Module. The maximum power draw is 25 Watts.

1.2.2 Specifications

Manufacturer:	AMD
Model:	Radeon E4690
Die name:	RV730 XT
Architecture:	Unified Superscalar Shader Architecture
Fabrication process:	55 nm
Transistors:	514 million
Bus interface:	PCIe 2.0 x16 (x4 or x8 as used on Agate)
Graphics clock frequency:	600 MHz
Memory specifications	
Size:	512 MB
Type:	GDDR3
Clock:	700 MHz
Clock (effective):	1400 MHz
Width:	128-bit
Bandwidth:	22.4 GB/s
Cores / Texture	
Color ROPs:	8
Stream processors:	320
Texture units:	32
RAMDACs:	2x RGB 10-bit DAC@400 MHz , 1x TV encoder
Decoders:	DivX, H.264, MPEG 1, MPEG-2, VC-1
Maximum power draw:	25 W
Digital resolution (max):	2@2048x1536 (2 displays max, Digital & VGA)
VGA resolution (max):	2@2048x1536
HDMI, HDCP:	***Not supported on Agate***
Performance	
Pixel fill rate:	4.8 Gigapixels/s
Texture fill rate:	19.2 Gigatexels/s
Single precision:	384 GFLOPS
Standards Support	
Open CL 1.0, OpenGL 3.3	
DirectX 10.1, Shader model: 4.1	
Linux, Windows XP-7	

1.3 E8860 Graphics Controller (Merlin)



1.3.1 Overview

The AMD Radeon E8860 embedded Graphics Processing Unit (GPU) consists of an advanced 3D graphics and multimedia engine with 2GB of high-speed GDDR5 frame buffer memory. With the memory clocked at 1 GHz, and using a 128-bit bus, the effective memory bandwidth is 64 GB/s.

The Graphics Core Next architecture is an advanced 3D graphics engine running at a core frequency of 625 MHz. It supports DirectX 11.1 and Shader Model 5.0 for superior graphics rendering. Its Unified Video Decoder (UVD) supports dual-stream High-Definition (HD) decode, as well as H.264 and VC-1 and entropy decode of MPEG-2 HD and MPEG-4 Part 2 (DivX and Xvid) content. The Video Compression Engine (VCE) supports the encoding of H.264 content. The E8860's HD audio controller and codec supports linear PCM and 7.1 channels of compressed HD audio.

The 640 shaders deliver 768 GFLOPs peak single-precision floating-point performance and 48 GFLOPs peak double-precision floating-point performance. Furthermore, it has 40 texture units, together with 16 color ROPs. The processing power is accessed through the an SDK, including the compiler, device driver, performance libraries and profiling tools.

AMD HD3D technology supports stereoscopic 3D graphics and 3D Blu-ray decode with a hardware multi-view decoder (MVC). AMD Eyefinity multi-display technology can drive up to six displays through integrated DisplayPort 1.1a/1.2, leveraging DisplayPort 1.2 for higher link speeds and multi-stream transport (MST) capabilities.

The E8860's intelligent PowerPlay technology optimizes power consumption with exceptional scalability of performance between 8W and 37W. The E8860 is produced in 28 nm technology and packaged as a 37.5mm square Multi-Chip Module (MCM) fine-pitch ball grid array (BGA). Host access is through the 16 lanes PCI Express 3.0 interface.

1.3.2 Specifications

Manufacturer:	AMD
Model:	Radeon E8860
Die name:	Venus (Adelaar)
Technology:	Graphics Core Next (GCN), AMD APP, AMD Eyefinity, and AMD HD3D, DirectCompute 11.1
Fabrication process:	28 nm
Transistors:	1.50 billion
Bus interface:	PCIe 3.0 x16 (PCIe 2.0 x4 or x8 as used on Merlin)
Graphics clock:	625 MHz
Memory specifications	
Size:	2048 MB
Type:	GDDR5
Clock:	1125 MHz
Clock (effective):	4500 MHz
Width:	128-bit
Bandwidth:	64.0 GB/s
Cores / Texture	
Compute units:	10
Color ROPs:	16
Stream processors:	640
Texture units:	40
RAMDAC:	1x triple 10-bit DAC, 400 MHz
Decoders:	Adobe Flash, DXVA 1.0 & 2.0, H.264, MPEG 2 (SH & HD), MVC (Blu-ray 3D), MPEG-4 Part 2 (DivX/Xvid), VC-1, WMV HD
HDMI, HDCP:	***Not supported on Merlin***
Digital resolution (max):	5@ 2560 x 1600, 1 @ 4096x2160 @60Hz DP1.2
VGA resolution (max):	1@2048 x 1536
Performance	
Pixel fill rate:	10.0 Gigapixels/s
Texture fill rate:	25.0 Gigatexels/s
Single precision:	768 GFLOPS
3DMark 11P Score	2689
Other features:	AMD: PowerTune, ZeroCore Power, PowerPlay, Direct Compute 11, HD3D Technology, High Dynamic Range (HDR)
Standards Support	Open CL1.2, OpenGL 4.3, DirectX 11.1, Shader model:5.0, Linux, Windows XP – 10

1.4 Comparison between E8860 and E4690

You might wonder why this section is here, especially since it makes the E8860-based Merlin look so much better than the E4690-based Agate. There are a couple of reasons:

a) the Merlin is targeted at multi-display systems and needs a higher performance graphics chip to drive as many as 6 displays at one time;

b) the Agate benefits from the lower power needs of the E4690 because is has a lot of other functions on the board.

Table 1-2 Feature Comparison between E8860 and E4690

Feature	E8860 (Merlin)	E4690 (Agate)
GPU die name	Venus	RV730
Memory clock speed	1,000 MHz	700 MHz
Effective memory clock speed	4,000 MHz	1,400 MHz
Memory bandwidth	64 GB/s	22.4 GB/s
Frame buffer memory	2 GB	512 MB
Memory type	GDDR5	GDDR3
Floating-point performance	736 GFLOPS	384 GFLOPS
Memory clock speed	1,000 MHz	700 MHz
Pixel rate	9.2 GPixel/s	4.8 GPixel/s
Texture Rate	23 GTexel/s	19.2 GTexel/s
Memory Bus	128 bits	128 bits
Shading units	640	320
Render Output Processors	16	8
Compute units	10	4
Texture mapping units	40	32
Graphics Clock Speed	625 MHz	600 MHz
Power Consumption	37W	25W

Table 1-3 GFXBench 3.0 Comparison between E8860 and E4690

Test *	E8860 (Merlin)	E4690 (Agate)
T-Rex Onscreen	3238 Frames (57.8 Fps)	3302 Frames (59.0 Fps)
T-Rex Offscreen	9863 Frames (176.2 Fps)	3906 Frames (69.8 Fps)
ALU Onscreen	1794 Frames (59.8 Fps)	1801 Frames (60.0 Fps)
ALU Offscreen	25220 Frames (420.3 Fps)	13800 Frames (229.8 Fps)
Alpha Blending Onscreen	12955 MB/s	4261 MB/s
Alpha Blending Offscreen	19715 MB/s	6235 MB/s
Driver Overhead Onscreen	1792 Frames (59.7 Fps)	1802 Frames (60.0 Fps)
Driver Overhead Offscreen	4873 Frames (81.2 Fps)	25027 Frames (417.1 Fps)
Fill Onscreen	15215 MTexels/s	7585 MTexels/s
Fill Offscreen	18510 MTexels/s	3014 MTexels/s
Render Quality MP	4549 mB PSNR	3756 mB PSNR
Render Quality HP	4549 mB PSNR	3756 mB PSNR

* Results courtesy gfxbench

1.5 Image Capture and Display Overview

Both the Agate and the Merlin contain some level of image capture capability, although to be sure, it is much more the focus of the Agate:

Table 1-4 AgatePXC Capture Capabilities

Feature	Typical Resolution	AgatePXC/2 Resource	Capture Format	Host interface
NTSC, PAL	720x480	Conexant CX25858	YUV	PCIe 1.1, x1
RGBHV or DVI or YUV	1600x1200	Analog Devices ADV7441A + Cypress FX3	YUV	USB 3.0 to PCIe 2.0 x1
		FX3 (ADV7441A disabled)		
MIPI CSI-2	2560x1536	Cypress CX3	YUV	USB 3.0 to PCIe 2.0 x1
USB 3.0 Rear I/O	n/a	uPD720201	n/a	USB 3.0 to PCIe 2.0 x1

Table 1-5 MerlinPXC Capture Capabilities

Feature	Typical Resolution	MerlinPXC/2 Resource	Capture Format	Host interface
MIPI CSI-2	2560x1536	Cypress CX3	YUV	USB 3.0 to PCIe 2.0 x1
USB 3.0 Front Panel	n/a	uPD720201	n/a	USB 3.0 to PCIe 2.0 x1
USB 3.0 Rear I/O	n/a	uPD720201	n/a	USB 3.0 to PCIe 2.0 x1

Table 1-6 MerlinMTX Capture Capabilities

Feature	Typical Resolution	MerlinPXC/2 Resource	Capture Format	Host interface
NTSC, PAL	720x480	Conexant CX25858	YUV	PCIe 1.1, x1

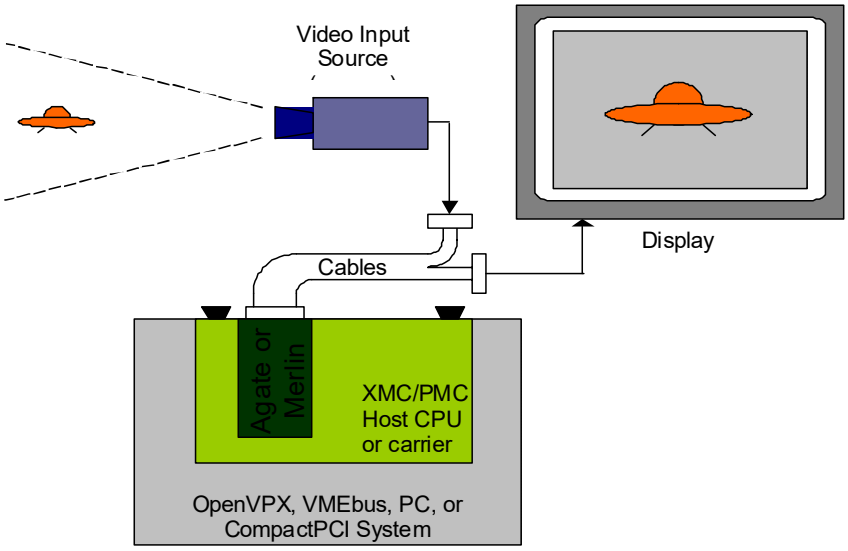
The “Host Interface” column details the way the capture data gets transported to the host.

Clearly, it is crucial for the AgatePXC and MerlinPXC that the host operating system have complete support for USB-video input. While this is not a problem for Windows or Linux, it militates against use of VxWorks, which doesn’t support UVC.

The E4690 and E8860 display controllers implement independent capture and playback software-based subsystems. Referring to the tables on the previous page, the relevant capture subsystem digitizes the video data and passes it on to a host-based capture buffer, usually in encoded YUV format.

The following diagram is a trivial sketch of how any capture/playback system is implemented.

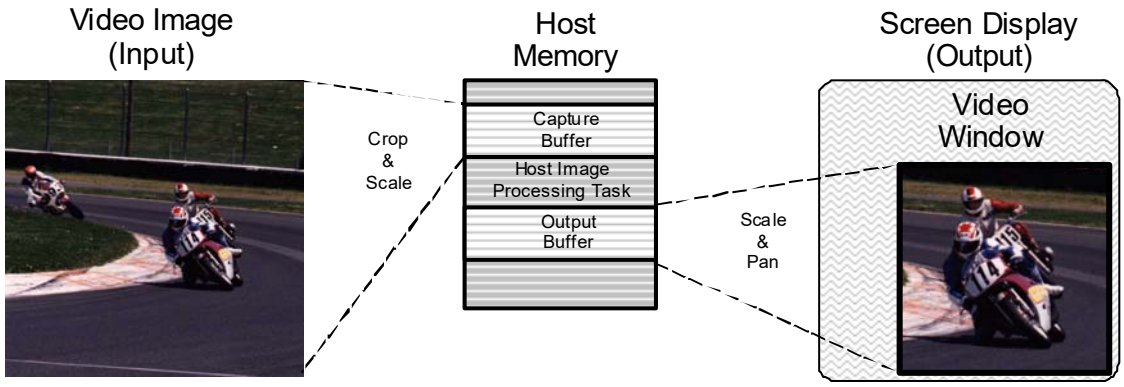
Figure 1-23 Silly Video Capture and Playback Support Diagram



Video Processing

Once in host memory, the video data may be archived for retrieval and display at a later time. Alternatively, the host CPU can perform a color space transform on the YUV data or extract the luminance in order to generate an 8-bit gray-scale image. Image enhancement algorithms may be applied in surveillance or monitoring applications, or edge-detection algorithms in automated (robotic) process control applications.

Figure 1-24 Capture to Display Path



Video Playback

Once the host has completed processing the image and has placed the data in an output buffer, the playback engine can retrieve it and incorporate it into the display output stream. The playback engine can up-scale (zoom) the contents of the video capture buffer before incorporating the capture image into the output stream. The image may either be made to fill the entire screen at the current resolution, or occupy a “window” within the larger output display. The window may be of arbitrary size and located on any pixel boundary. Color keying may be used to create non-rectangular windows, and/or to superimpose a graphics overlay on the video image.

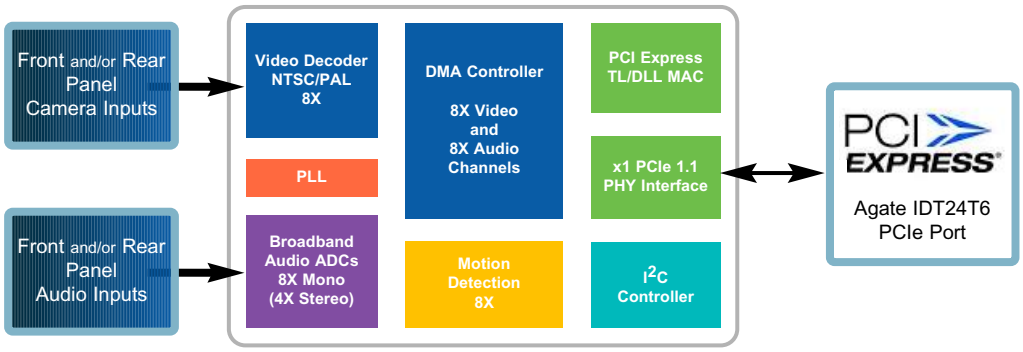
1.6 CX25858 8-Channel NTSC/PAL & Audio Digitizer

1.6.1 Overview

The CX25858 8-Channel Audio/Video Decoder with Integrated PCIe Interface contains eight high quality NTSC/PAL video decoders with 10-bit A/Ds and 5-line comb filtering, to generate the highest quality digital video output with the lowest possible noise. This creates not only the best image quality for viewing, but enables lower bit rates for compression devices using the output of the CX25858. The video decoders within the CX25858 are optimized to lock to inputs with low signal levels as well as line-locked cameras, both of which are common in surveillance systems. Each video decoder may be scaled independently and the CX25858 supports BT.656 as well as a variety of other interleaved digital video output formats.

The CX25858 includes programmable motion detection logic, which can trigger interrupts over the PCIe bus when motion is detected on incoming analog video streams. ***Please see note in Section 1.1 regarding PMC.***

Figure 1-25 CX258585 Video Digitizer Block Diagram



1.6.2 PCIe Bridging

The CX25858 has a PCIe 1.1 compliant x1 subsystem which contains the interfaces, data buffers, and control registers to enable high bandwidth data transfers between the CX25858 and the host. Features have been incorporated to accommodate PCIe bus latencies and minimize data loss.

Data is buffered internally and is transferred using a RISC DMA Engine which maximizes use the PCIe's 2.5 Gbps bandwidth to stream up to eight channels of data to host memory at any time. Each DMA channel is programmed with a set of RISC instructions generated by the OS driver that specify PCIe address locations and sync to incoming data streams.

1.6.3 10-bit NTSC/PAL Video Decoders

Each of the CX25858 eight video inputs has a 10-bit Analog to Digital Converter (ADC). All video inputs have integrated anti-alias filters, eliminating the need for external filter components. DC restoration and Automatic Gain Control (AGC) are provided to compensate for the sources with differing average picture levels. Manual gain control is also supported.

1.6.4 High Performance Y/C Separation

Luma/chroma separation of composite video sources is accomplished through a 5-line adaptive chroma comb filter which determines which of the five lines are appropriately correlated enough to average together. Depending upon the amount of correlation among the lines, two or three lines averaged together result in a combed filtered line.

In the case where no correlation exists between the lines, the CX25858 automatically falls back to chroma band-pass and luma notch filtering The output of the chroma comb filter is also re-modulated and fed back into the luma channel. The result is a high quality image with reduced cross-chrominance and cross-luminance artifacts, such as dot crawl, hanging dots, and rainbow effects that restore full bandwidth to luminance data from composite sources.

1.6.5 Video Processing Functions

Back-end video processing functions include contrast, brightness, hue, saturation, and scaling. In addition, the luma data path provides white crush compensation for sources that exceed sync tip to white level ratios. The CX25858 also provides four sets of selectable peaking filters for sharpening the image. The luma data output range is selectable so that luma codes can be limited to the nominal ITU-R BT.656 code range, or can support values below black level. Additional chroma functions include AGC to compensate for attenuated color subcarriers, a color killer for true black and white sources, and coring for limiting low-level chroma noise.

1.6.6 High Quality Scaling

The CX25858 can downscale digital video from 16-bit per pixel 4:2:2 format to12-bit 4:1:1 format or 8-bit Y8. Data can be transferred to host memory in Packed or Planar format.

Arbitrary horizontal and vertical scaling is available, from full resolution down to an 8:1 ratio (icon size). To maintain a high quality scaled image, multi-tap 64-phase interpolation is used. The horizontal luma scaler uses 6-tap FIR interpolation between horizontal source samples, while the horizontal chroma scaler uses 4-tap interpolation. Line store memory is integrated into the CX25858 so that the vertical scaler-depending on the

horizontal scaling ratio-can use from 2-tap to 5-tap, seven phase interpolation between lines. Each video decoder has both scaled and non-scaled outputs that can be independently interleaved with other sources.

1.6.7 Fast Locking Algorithm

Another distinguishing feature of CX25858 is its fast locking algorithm which locks onto the first vsync that it encounters, regardless of its position, whereas the normal vertical locking algorithm (1'b0) looks for a sync within an expected window. If no sync appears during the next expected window, it locks onto the first subsequent incoming vsync.

The fast locking algorithm bypasses the 8-field hysteresis that is built into the field detection logic. In this mode, as soon as the even/odd field is detected, the field signal reflects the status. When fast locking is disabled, the field detection must be stable for eight consecutive fields before the field signal reflects the change. The CX25858 will lock vertically to a switched input signal in less than 1 field, regardless of the relative timing between the original and new signals.

1.6.8 Camera ID and Time Stamp Insertion

Each video decoder can optionally insert a unique Camera ID into the first Active Line, the HBI, and/or the Hamming code field of the SAV/EAV codes of the video output stream. This can be used by the codec or other receiver to de-interleave lines and frames. The decoders can also optionally insert a Reference Time Code (RTC) generated by the audio PLL clock for A/V Syncing by the codec.

1.6.9 Audio ADCs

The CX25858 has four Stereo Audio ADCs for eight mono channels of analog audio input. The Audio ADCs each support 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz audio sample rates, up to 20 kHz input bandwidth, an integrated anti-alias filter, and programmable analog and digital gain.

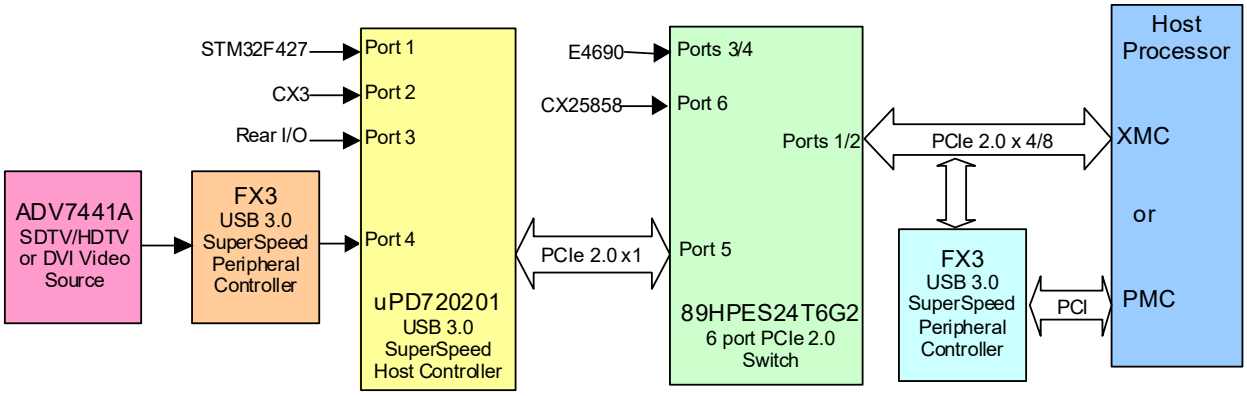
1.6.10 Additional Features

The CX25858 includes programmable motion detection logic, which can trigger flags or PCIe interrupts when motion is detected on incoming analog video streams. The CX25858 contains an I^2C interface for the startup EEPRPOM code.

1.7 ADV7441A RGBHV/DVI Digitizer (Agate)

The ADV7441A performs the front-end RGBHV and DVI processing for the high resolution acquisition subsystem on the Agate. Please refer to the block diagram on the following page. Also, please refer to data path diagram (below) which shows how the 7441A fits into the Agate design.

Figure 1-26 DVI/RGBHV Digitizer Data Path



1.7.1 Introduction

The ADV7441A is a high quality, single-chip, multiformat video decoder and graphics digitizer with an integrated DVI receiver.

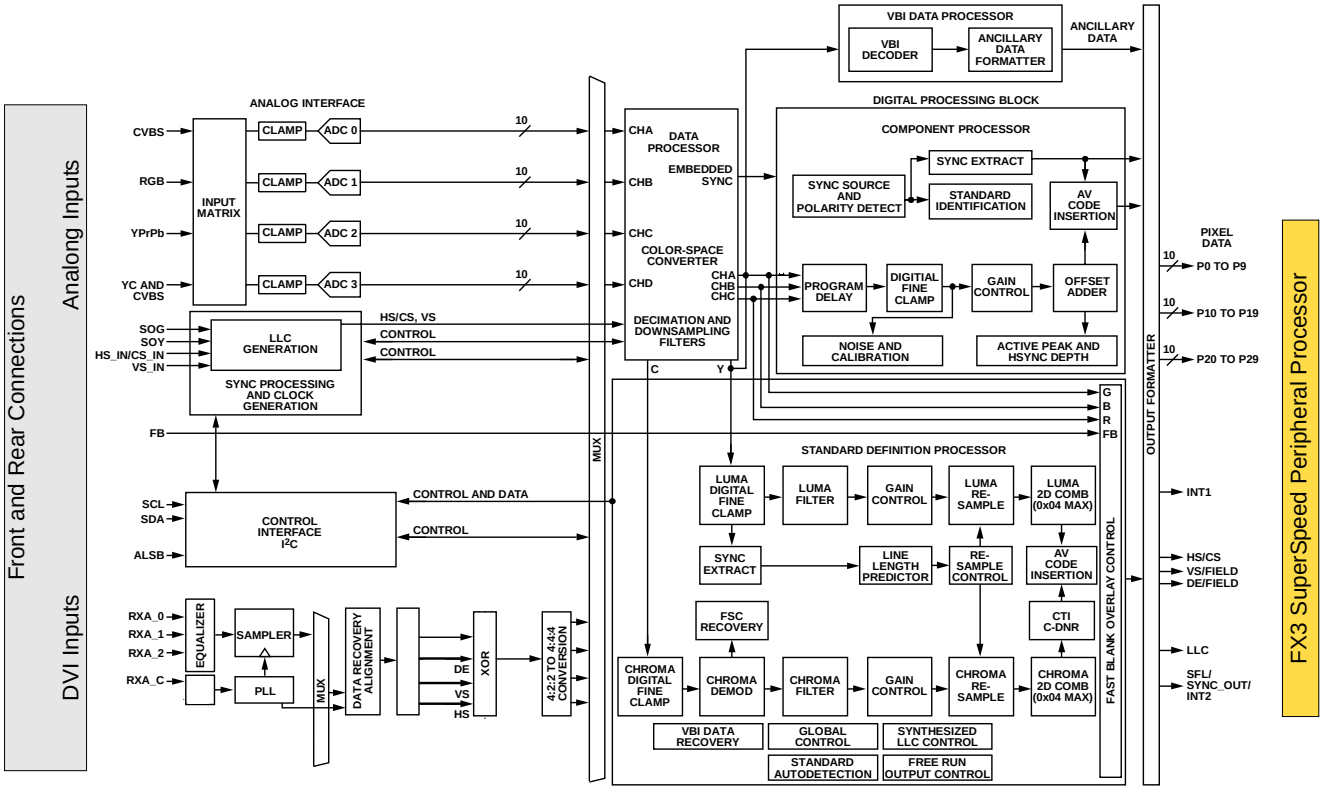
The ADV7441A contains two main processing sections:

1) The first section is the standard definition processor (SDP), which processes all types of PAL, NTSC, and SECAM composite or S-video signals into a digital ITU-R BT.656 format. It can also decode a component RGB or YPrPb video signal into a digital YCrCb or RGB pixel output stream. The device supports the 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and 1250i component video standards as well as many other HD and SMPTE standards.

2) The second section is the component processor (CP), which processes YPrPb and RGB component formats, including RGB graphics from VGA to UXGA rates and convert them into a digital RGB or YCrCb pixel output stream.

   The CP also processes the video signals from the 225Mhz DVI receiver, supporting formats up to 1080p and display resolutions up to UXGA.

Figure 1-27 ADV7441A DVI/RGBHV Digitizer Block Diagram



1.7.2 Analog Front End

The ADV7441A analog front end comprises four 10-bit 170 MHz Noise Shaped Video ADCs that digitize the analog video signal before applying it to the CP or SDP. The analog front end employs differential channels to each ADC to ensure high performance in a mixed signal application. The front end includes an input mux that enables multiple video signals to be applied to the ADV7441A. It also includes optional internal anti-aliasing filters with approximately 6 MHz bandwidth.

Current and voltage clamps are positioned in front of each ADC to ensure the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping in the CP. The ADCs are configured to run in 4X oversampling mode when decoding component 525i, 625i, 525p, and 625p sources. All other video standards are 1X oversampled. In oversampling the video signals, a reduction in the cost and complexity of external anti-aliasing filters can be obtained with the benefit of an increased signal to noise ratio (SNR).

1.7.3 Standard Definition Processor

The SDP section can automatically detect and process a large selection of baseband video signals in composite, S-Video, and YUV formats including PAL B/D/I/G/H, PAL60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L.

The SDP has a 5-line super-adaptive 2D comb filter that gives superior chrominance and luminance separation. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality. The SDP has an IF filter block that compensates for attenuation in the high frequency luma spectrum due to tuner SAW filter. The SDP has specific luminance and chrominance parameter control for brightness, contrast, saturation, and hue.

The ADV7441A implements an Adaptive Digital Line Length Tracking algorithm to track and decode poor quality video sources. The SDP also contains a Chroma Transient Improvement processor which increases the edge rate on chroma transitions, resulting in a sharper video image.

1.7.4 Component Processor

The CP section accepts video data from the analog front end or from the DVI receiver. Component video standards supported by the CP include 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, 1250i, VGA up to UGA at 60 Hz, and many other standards.

The ADV7441A includes a fully programmable any-to-any 3 x 3 color space conversion (CSC) matrix. This enables YPrPb to RGB and RGB to YCrCb conversions of video data coming from the analog front end or the DVI receiver. Many other standards of color space can be implemented using the color space converter.

The CP also contains an AGC block. In cases where no embedded synchronization is preset, the video gain can be set manually. The AGC section is followed by a digital clamp circuit that ensures the video signal is clamped to the correct blanking level. Manual and automatic adjustments within the CP include gain (contrast) and offset (brightness).

The video data coming from the DVI receiver is routed through the Data Preprocessor (DPP) and then into the CP block. This video path allows for a high level of control and processing over the video data before it is output on the pixel and synchronization ports.

1.7.5 VBI Data Processor

The VBI Data Processor (VDP) can slice and decode VBI data from the incoming CVBS/YC/YUV processed by the SD core. It can also decode VBI data on the luma channel of the YUV data processed by the CP
The VDP supports the following VBI data standards.

1.8 FX3 SuperSpeed Peripheral Controller (Agate)

The Cypress FX3 is a USB 3.0 SuperSpeed peripheral controller, providing integrated and flexible features. The FX3 has integrated the USB 3.0 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications.

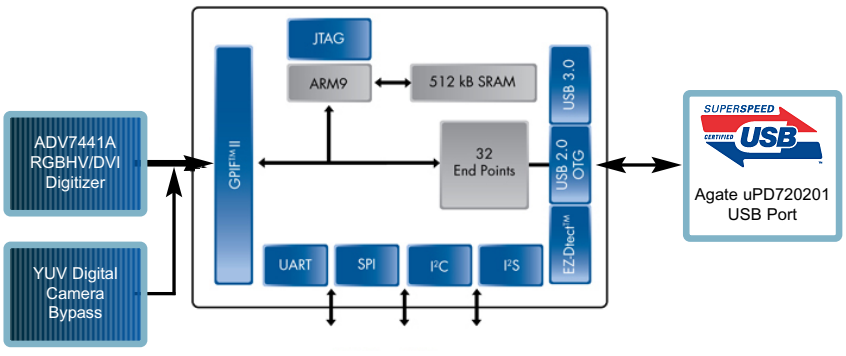
The FX3 has a fully configurable, parallel, general programmable interface called GPIF II enables 375-MBps data transfer from GPIF II to the USB 3.0 interface.

The FX3 contains 512 KB of on-chip SRAM for code and data. The FX3 also provides interfaces to connect to serial peripherals including the external SPI serial boot PROM and an I^2C port for controlling the ADV7441A. The FX3 provides a JTAG port for debugging which is accessible on the Agate via an optional 3-pin 2mm header.

The Agate links to the ADV7441A (see Section 1.7) or a YUV camera to the FX3 following the Cypress AN75779 UVC Video Interface Application Note, which includes setup for the GPIF and code examples. Cypress also provides FX3 with an SDK and other development tools for use under Windows and Linux.

It turns out that the programming interfaces for most of the YUV cameras are largely proprietary. This makes it difficult to obtain sufficient register information to correctly program the cameras and set up the FX3. For this reason, Rastergraf has chosen a demo setup that has a camera and firmware that is known to work with the FX3. See the Applications section later in this manual for more information.

Figure 1-28 FX3 SuperSpeed Peripheral Controller Block Diagram



1.9 CX3 MIPI Controller (Agate/MerlinPXC)

Cypress's EZ-USB CX3 connects devices with MIPI CSI-2 (Mobile Industry Processor Interface – Camera Serial Interface 2) interface to a port on the Agate or Merlin uPD720201 USB 3.0 host controller.

CX3 has a 4-lane CSI-2 receiver with up to 1 Gbps on each lane. It supports video data formats such as RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit.

CX3 has integrated the USB 3.0 and USB 2.0 physical layers along with a 32-bit 200-MHz ARM926EJ-S core CPU. The core has direct access to 16 KB of Instruction Tightly Coupled Memory (TCM) and 8 KB of Data TCM. The CX3 provides a JTAG port for debugging which is accessible on the Merlin and Agate via an optional 3-pin 2mm header.

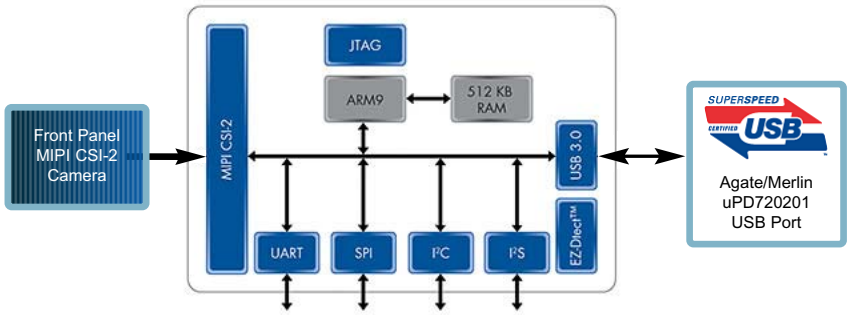
The CX3 integrates 512 KB of embedded SRAM for code and data. It implements efficient and flexible DMA connectivity between the USB and CSI-2 port requiring firmware only to configure data accesses.

Examples of the CX3 firmware are available with the Cypress EZ-USB CX3 Software Development Kit (SDK). APIs that can be ported to the host OS are included in SDK.

It turns out that the programming interfaces for both MIPI and most of the MIPI cameras are largely proprietary. While they are MIPI hardware compatible, there is no such thing as a compatible register set. Even within one manufacturer, there is little consistency.

This makes it difficult to obtain sufficient register information to correctly program the cameras and set up the CX3. Also, another feature of MIPI cameras is that while they are MIPI compatible, For this reason, Rastergraf has chosen a demo setup that has a camera and firmware that is known to work with the CX3. See the Applications section later in this manual for more information.

Figure 1-29 CX3 MIPI Controller Block Diagram



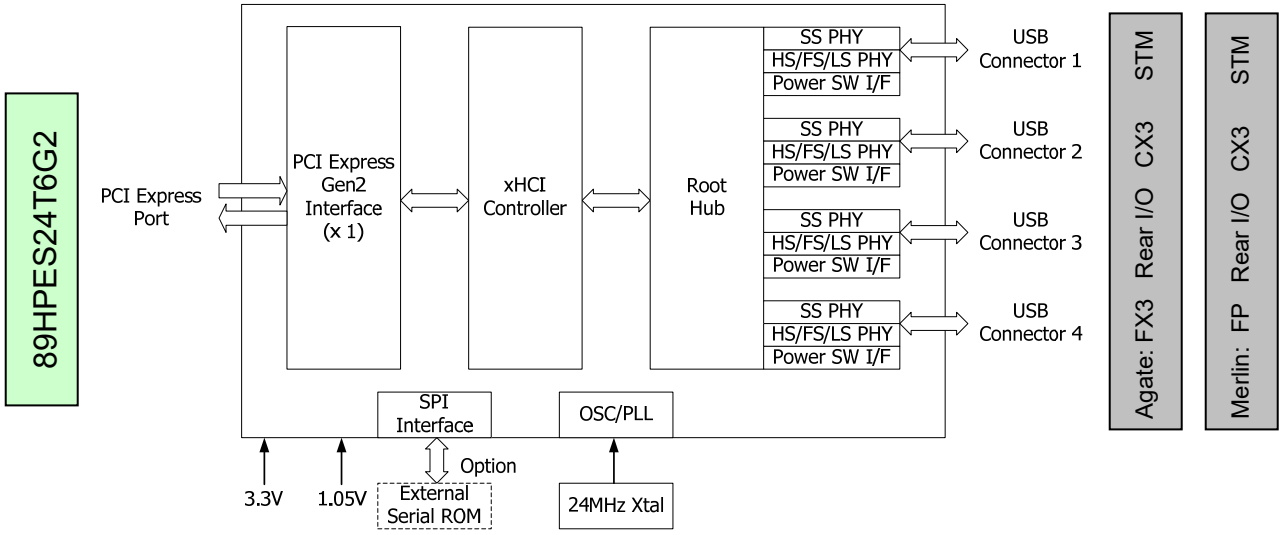
1.10 uPD720201 USB 3.0 Host Controller (Agate/MerlinPXC)

The µPD720201 supports four USB3.0 SuperSpeed ports. The µPD720201 uses an x1 PCI Express Gen 2 system interface bus. On power-up, it loads its firmware from a Serial Peripheral Interface (SPI) type ROM.

When connected to USB 3.0-compliant peripherals, the µPD720201 can transfer information at clock speeds of up to 5 Gbps. The µPD720201 is backwards compatible with the older USB2.0 standard which supports the Low-Speed (1.5 Mbps), Full-Speed (12 Mbps), and Hi-Speed (480 Mbps).

As used on the Agate and Merlin, the uPD720201 ports are used for the debugger port on the STM32F427 BIST processor, front and/or rear access ports, and the Cypress USB peripheral processor(s).

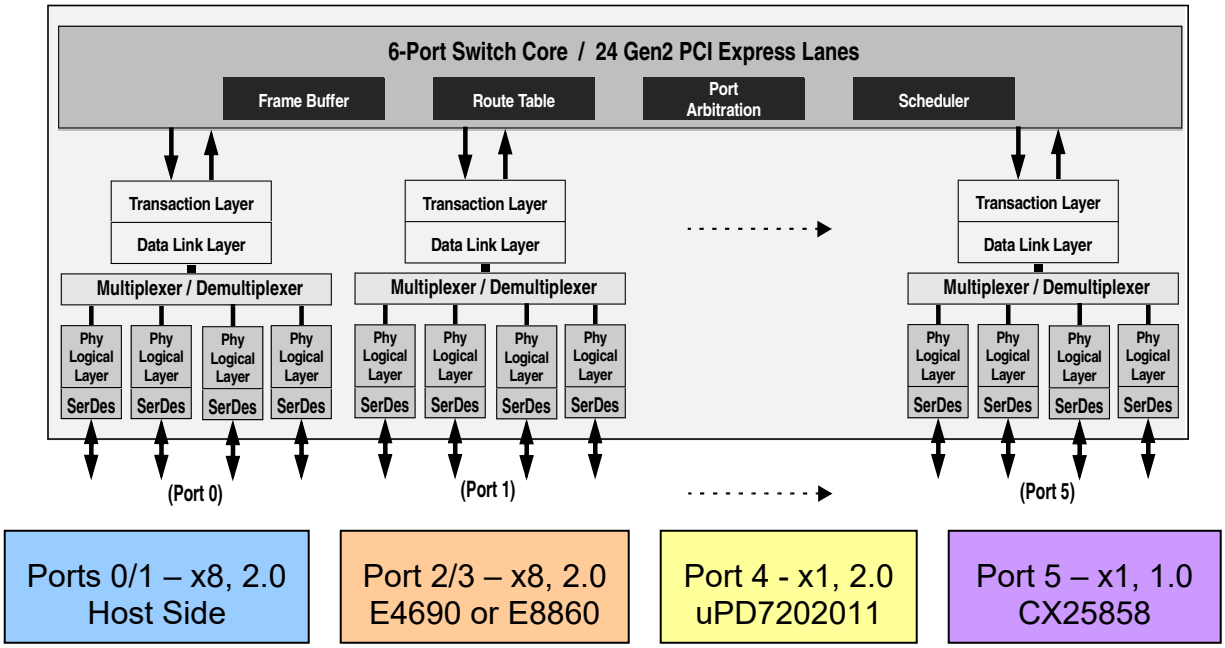
Figure 1-30 uPD720201 Host Controller Block Diagram



1.11 89HPES24T6G2 PCIe 2.0 Switch

Utilizing standard PCI Express interconnect, the PES24T6G2 provides connectivity for up to 6 ports across 24 integrated serial lanes. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCIe 2.0, including operation at 5 Gbps, 2.5 Gbps, and mixed 5 Gbps/2.5Gbps modes.

Figure 1-31 89HPES24T6G2 PCIe 2.0 Switch Block Diagram



Note: x1 or x8 = PCIe lane width. 1.0 xfr speed = 2.5Gb/s, 2.0 xfr speed = 5 Gb/s.

The PES24T6G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCIe 2.0. The PES24T6G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching.

The PES24T6G2 contains two SMBus interfaces. The slave interface is provides full access to the configuration registers in the PES24T6G2, allowing every configuration register in the device to be read or written by the host CPU or the local STM32F427 BIST processor. The master interface allows the default configuration register values to be overridden following a reset with values programmed in an external serial EEPROM.

1.12 Flexible Display Support

1.12.1 Overview

The graphics boards support a variety of displays, including DisplayPort, VGA, LVDS, and DVI panels. Using in-line dongle adapters, you can convert from DisplayPort to DVI, HDMI, VGA, or NTSC. This flexibility enables the boards to be incorporated into a wide variety of applications.

The main practical differences between the Agate and the Merlin involve the kind and number of display channel choices that are available:

Versions of the Agate provide front panel access to DisplayPort, VGA, or LVDS and a variety of rear panel options. You can only have to 2 active display channels at one time.

MerlinPXC versions provide front panel access to 4x DisplayPorts or a single VGA and a variety of rear panel options. You can have up to 6 active display channels at one time.

MerlinMTX provides 2 DVI and 1 DisplayPort on the rear I/O PMC Pn4 connector. You can have all 3 display channels active at one time.

Table 1-7 Display Options for Agate and Merlin

Board Model	Total Active Channels	Front Panel *	Rear
AgatePXC/1V	2	2x VGA	2x VGA, 2 DisplayPort
AgatePXC/1D	2	2x mDP	2x VGA, 2 mDP
AgatePXC/1L	1	1x LVDS	2x VGA, 2 mDP
AgatePXC/2	2	2x mDP, 1x I/O	2x VGA, 2 mDP
MerlinPXC/1V	6	1x VGA	3 DisplayPort
MerlinPXC/1D	6	4x mDP	1x VGA, 3 mDP
MerlinPXC/2	6	4x mDP, 1x USB, 1xMIPI	1x VGA, 3 mDP, 1x USB
MerlinMTX	3	--	2 DVI, 1 mDP

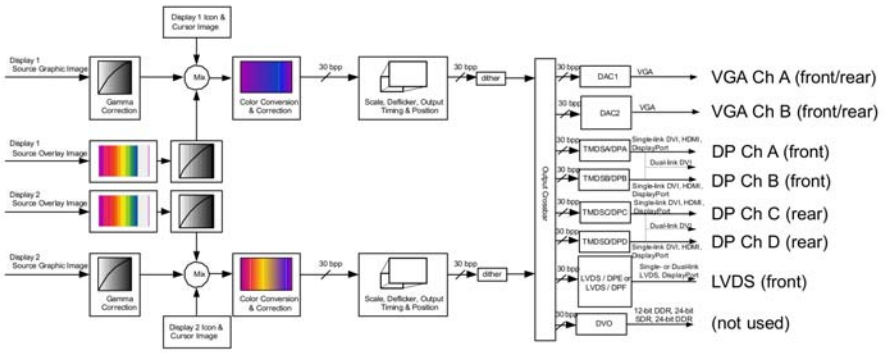
* *Notes: mDP = DisplayPort using Mini DisplayPort connector*
Merlin supports only one VGA channel

1.12.2 Agate Display Controller Features

The E4690 contains dual fully featured, symmetrical and independent display controllers that support true 30-bpp throughout the display pipe. They support for display resolutions up to 3840x2400 per display output, which does not oversubscribe available memory bandwidth.

Each controller contains advanced video capabilities, including high fidelity gamma, color correction and scaling, adaptive per-pixel de-interlacing and frame rate conversion (temporal filtering).

Figure 1-32 E4690 Display Channels



Remember that for Agate, only two outputs can be active at one time.

1.12.2.1 DisplayPort Features

The E4690 supports up to four Version 1.1a DisplayPorts. The dual front panel connectors (on the AgatePXC /1D and /2 versions) use standard Mini DisplayPort connectors. The rear connections are made via the Pn6 XMC connector which can be accessed through the AgatePXC PIM rear I/O breakout board.

Using the DDC/AUX control lines, the OS can determine the monitor connection and capabilities. Each DisplayPort link can support options for the number of lanes and link data rate as follows:

Table 1-8 Maximum pixel rates for 4, 2, or 1 lane(s) at 2.7-GHz link rate

Lane(s)	18 bpp	24 bpp	30 bpp	Typical Resolution
1	119 MPixs/s	89 MPixs/s	71 MPixs/s	
2	239 MPixs/s	179 MPixs/s	143 MPixs/s	1920x1200@60Hz
4	359 MPixs/s	359 MPixs/s	287 MPixs/s	2560x1600@60Hz

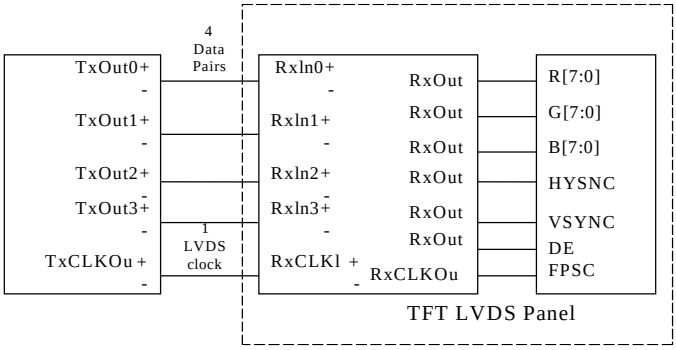
1.12.2.2 LVDS Features

The AgatePXC/1L provides an LVDS output on the front panel via a 26-pin Mini Camera Link compatible SDR connector. It is ANSI/TIA/EIA-644 and FPDI-2 compliant and is compatible with receivers from National Semiconductor, Texas Instruments, and THine. LVDS encoding can be supplied in either VESA or LDI format.

Taking output from either of the internal display controllers, LVDS output supports a single-link (or channel) or dual-link LVDS transmitter. It can drive either 18-bpp (3 data +1 clock pairs) or 24-bpp (4 data +1 clock pairs) displays with several dithering options from the internal 30-bpp display controller. It also supports ratiometric expansion and compression on panels with reduced blanking.

The LVDS encoder operating in single-link (or channel) 24-bit mode compresses 24 bits of RGB data and 4 bits of LCD timing into four differential wire pairs, up to 392 MB per second at a maximum clock rate of 112 MHz. A fifth differential pair transmits the interface clock. This mode supports up to SXGA+ panel (1400x1050x24 @60Hz).

When operating in dual-link (or channel) mode, the encoder provides two pixels per clock. An additional 4 our differential wire pairs are used to supply the second encoded pixel. In this mode, the LVDS port can be used



to drive a panel of up to QXGA size (2048x1536)

Figure 1-33 LVDS Single Link Flat Panel Output Block Diagram

1.12.2.3 Dual Analog Output Features

The E4690 provides two integrated triple 10-bit DACs. Each DAC takes output from the primary or secondary internal display controller or the internal analog TV encoder (DAC2 only). The resulting output is RGB at a maximum pixel frequency of 400 MHz. Using the DDC control lines, the OS can determine the monitor connection and capabilities.

1.12.2.4 TV Out (on DAC2) Features

Available only on DAC 2, the E4690 provides an Internal CE class TV encoder for YPrPb, NTSC and PAL (all variants supported). It can take its input from either internal display controller and drive the output on DAC2.

Available output modes include: component YPrPb for 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p, YC S-video output for NTSC & PAL, and single wire composite output for NTSC & PAL.

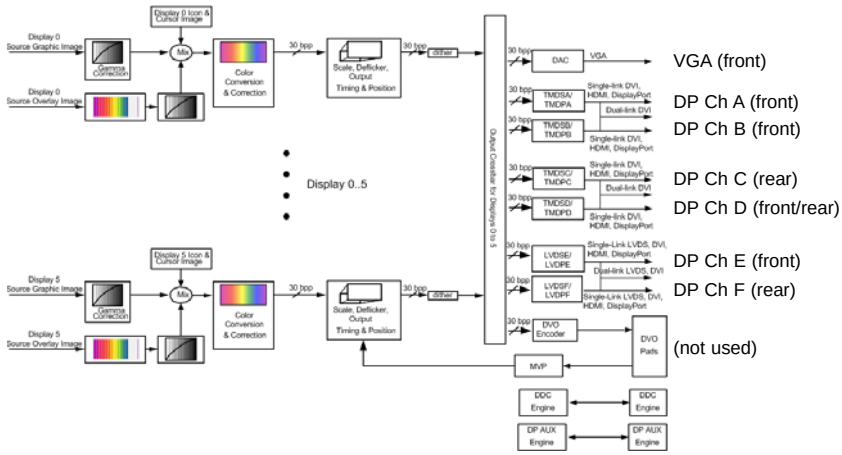
The TV Encoder supports underscan in all TV modes, scaling and internal adaptive flicker filtering for interlaced TV outputs, and two line comb-on-the-way-out for luma-chroma cross-talk prevention. It is capable of supporting the VBI data insertion for NTSC, PAL, and SECAM.

1.12.3 Merlin Display Controller Features

The E8860 contains six fully featured, symmetrical and independent display controllers that support true 30-bpp throughout the display pipe. They support for display resolutions up to 4096×2160@30 Hz per display output, which does not oversubscribe available memory bandwidth.

Each controller contains advanced video capabilities, including high fidelity gamma, color correction and scaling, adaptive per-pixel de-interlacing and frame rate conversion (temporal filtering).

Figure 1-34 E8860 Display Channels



Remember that for Merlin, six outputs can be active at one time and there is only one VGA output.

1.12.3.1 DisplayPort Features

The E8860 supports up to six Version 1.2 DisplayPorts. The four front panel connectors (on the MerlinPXC /1D and /2 versions) use standard Mini DisplayPort connectors. The rear connections are made via the Pn6 XMC or Pn4 PMC connector which can be accessed through the MerlinPXC PIM rear I/O breakout board. With the use of both the front and rear connections, it is possible to have all 6 channels active at once.

Perhaps the coolest feature of the E8860 DisplayPort controller is DisplayPort Multi-streaming Transport (MST), which enables any number of display pipelines to drive a single DisplayPort interface (provided the DisplayPort link bandwidth is not exceeded). This means that you can drive several monitors through one DisplayPort output, provided the monitors also support MST.

Using the DDC/AUX control lines, the OS can determine the monitor connection and capabilities. Each DisplayPort link can support options for the number of lanes and link data rate as follows:

Table 1-9 Maximum pixel rates for 4, 2, or 1 lane(s) at 2.7-GHz link rate

Lane(s)	18 bpp	24 bpp	30 bpp	Typical Resolution
1	119 MPixs/s	89 MPixs/s	71 MPixs/s	
2	239 MPixs/s	179 MPixs/s	143 MPixs/s	1920x1200@60Hz
4	359 MPixs/s	359 MPixs/s	287 MPixs/s	2560x1600@60Hz

Table 1-10 Maximum pixel rates for 4, 2, or 1 lane(s) at 5.4-GHz link rate

Lane(s)	18 bpp	24 bpp	30 bpp	Typical Resolution
1	240 MPixs/s	180 MPixs/s	144 MPixs/s	
2	480 MPixs/s	360 MPixs/s	288 MPixs/s	2560x1600@60Hz
4	597 MPixs/s	597 MPixs/s	576 MPixs/s	4096x2160@60Hz

1.12.3.2 Single Analog Output Features

The E8860 provides a single integrated triple 10-bit DAC. The DAC takes output from the primary or secondary internal display controller. The resulting output is RGB at a maximum pixel frequency of 400 MHz. Using the DDC control lines, the OS can determine the monitor connection and capabilities.

Note that in its infinite wisdom, AMD omitted the TV encoder from the E8860. This means that if you want TV output, you will need to use an external TV encoder box.

1.12.3.3 DVI Output Features

Several of the E8860 DisplayPort outputs can be reconfigured to provide DVI output instead. The MerlinMTX makes use of DP Channels D and F to provide single-link (1920x1200) DVI ports on the PMC Pn4 connector.

1.13 STM32F427 Integrated System Monitor (ISM)

1.13.1 Overview

The ST Micro STM32F427 is based on the high-performance ARM Cortex-M4 32-bit RISC core operating at 180 MHz. It incorporates 2MB Flash and 256 KB SRAM.

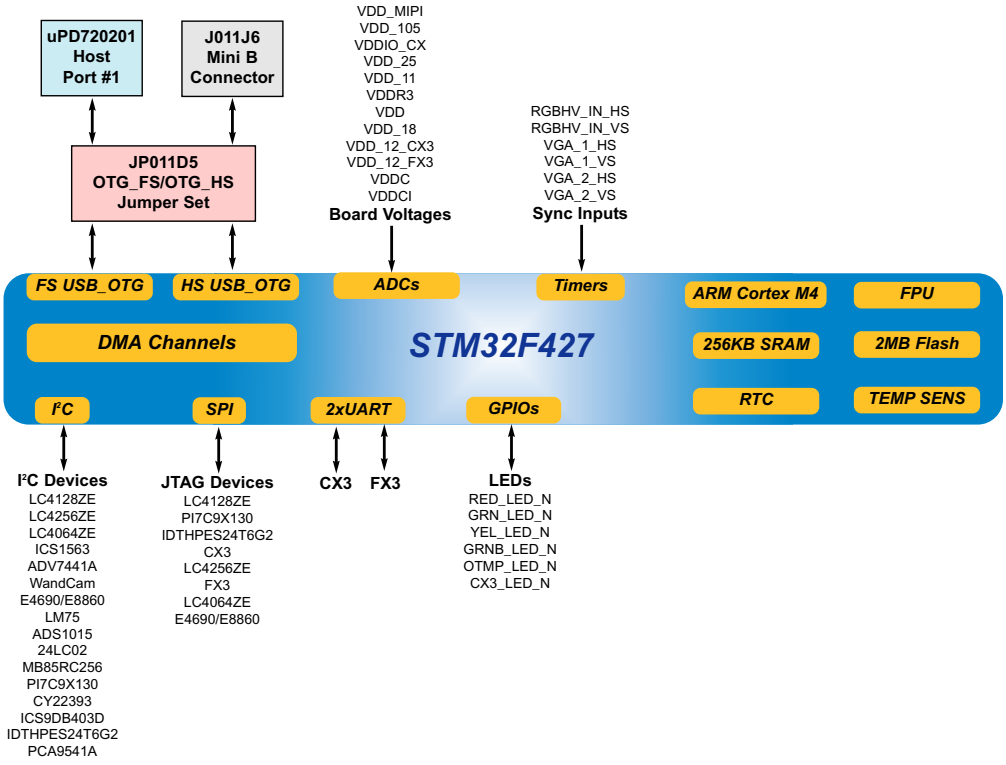
1.13.2 Using the STM32F427 on the Agate or Merlin

The STM32F427 CPU functions as an Integrated System Monitor (ISM and provides for the Agate and Merlin both Built-In Self-Test (BIST) capabilities and real-time monitoring of many device functions using a combination of I^2C, JTAG, and A/D converters (voltage measurements).

The STM firmware includes boot-time register setup, device testing, and CPLD reprogramming. You can connect to the ISM via the Mini B connector on the edge of the Merlin and using a host USB port.

Please refer to Section 3.10.2 for information about connecting to the ISM USB port. Please refer to Section 6.3 for information about how to use the ISM. Please refer to Section 8.8 for information about the software needed to connect to the ISM.

Figure 1-35 STM32F427 Utilization



1.13.3 System Management Connections

A Mini B USB connector located on the edge of the board enables access to the STM secondary USB port for use:

a) with USB peripheral devices including memory sticks and keyboards;

b) as the primary means for accessing the ISM firmware. When correctly jumpered and using an ST Micro Windows USB port driver, you can access the STM firmware via a host system USB port with HyperTerminal or PuTTY. See Section 8.8 for more information.

A Micro AB USB connector is used (for convenience) for access to the STM SWD debug port. It is NOT a USB port and is ONLY to be used to update the ISM firmware. See Section 3.10.1 for more information.

1.13.4 Implementing the STM32F427 Resources

The following table shows how the STM32F427 resources are utilized on the Agate and Merlin. Understand that this is not all that the chip can do, but only because a number of its features are not applicable to the overall intent of the Agate and Merlin.

Table 1-11 STM32F427 Feature Utilization

STM23F427 Feature	As Utilized on Agate or Merlin
2MB Flash	Firmware Storage
256 KB SRAM	Working memory for Firmware and USB Ports.
RTC	task control
timers	track HSYNC and VSYNC timing for VGA outputs (not MerlinMTX) and RGBHV input (Agate only)
Analog mux to ADCs	Measure a wide variety of board voltages
SWD debug interface	Supports firmware download and debug
82 5V-tolerant I/Os	Includes all non-power or clock pins. See Section 2.6 and Section 2.7 for I/O allocations
I^2C/SMBus interface	Access many on-board devices - see Section 2.5.3
2 UARTs	STM runs terminal emulators to help enable user debug for CX3 (not Merlin MTX) and FX3 (Agate only)
SPI interface	Used as JTAG controller to interrogate all on-board JTAG-enabled devices - see Section 2.5.2
2x USB ports	See Section 3.9.2
100 pin TQFP package	It fits

1.14 System Elements (Agate/Merlin)

There are a number of other subsystems besides the ISM on the graphics board that are required to enable its correct and reliable operation.

1.14.1 Power Supply Subsystem

By the very definition of a high-performance graphics board, these boards are not low-power designs. The estimated power requirements are:

Host Bus	Voltage Input	Idle	Peak (1s) Operation
PMC/XMC	3.3V	~0.9A	~2A
PMC	5V	~2.45A	~6.85A
XMC	VPWR=5V	~2.45A	~6.85A
	VPWR=12V	~1.1A	~3A

If you fiddle with the overclock settings in the Catalyst Control Panel, it may be possible to exceed these ratings. Please consult with Rastergraf before trying to run the graphics chip at the higher clock speeds.

The startup of the power systems is set in motion by the leading edge of the system reset pulse. All host power must be stable at that time in order to ensure the proper operation of the board. Logic selects PMC or XMC as the power source (XMC is default). Because it can deliver the most power, 5V is the power rail for the multi-phase DC-DC converter supply which supplies the many sub-3.3V supplies needed on the board..

When XMC VPWR=12V, a local DC-DC converter is enabled to down-convert it to 5V. There is small efficiency cost to doing this but it simplifies the overall design. An OVP shuts down the entire power section if local 5V exceeds 5.6V.

FET switches select the source of the 5V between PMC, XMC when it is 5V, and the local down-converter. Each FET switch measures the current through its load pin, and this can be reported to the system via the ISM..

1.14.2 Temperature Monitoring Subsystem

An LM75 sensor monitors the DC-DC converters area.

An LM63 tied remotely to the GPU substrate diode monitors the die temperature as well as its own internal sensor. Since the LM63 is located a small distance from the GPU, it can provides thermal gradient data. The LM63 is monitored by the graphics chip software as well as the ISM.

The STM32F427 itself contains a temperature sensor.

Since the four sensors are located in different areas of the board, some simple thermal profiling of the board can be performed. Also, if a thermal condition is detected, an LED is lit and, if required, the board is shut down. Recovery is done by cycling system power.

1.14.3 Cooling Systems

Copper floods enhance the heat-spreading within the PCB. The 24T6 and E8860 PCIe bus widths (set on-board to x4 or x8) and the GPU clock and core voltage also affect power dissipation by a significant amount. The BIST subsystem can adjust the GPU parameters when temperatures rise too high. This may be a more effective way to manage heat than adding a heat sink that may congest the air flow through the cardcage. Tests will have to be run in the customer system to determine the impact.

That said, the AgatePXC and MerlinPXC are shipped with a low-profile heat spreader/sink that does make a significant difference in operating temperature of the GPU when some air flow is applied across the board.

1.14.4 STM32F427 Integrated System Monitor (ISM)

As mentioned in Section i.13, the STM32F427 CPU provides for the Agate and Merlin both Built-In Self-Test (BIST) capabilities and real-time monitoring of many device functions using a combination of I^2C, JTAG, and A/D converters (for voltage measurements). See Section 1.13 for information about the STM32F427 and its use in the Agate and Merlin. See Section 6.3 for information on how to use the ISM.

1.14.5 LED Error Reporting (Agate)

On the AgatePXC/2 front panel are:

- Green “ST” LED driven by the STM, slowly cycles on and off.
- Green “VOK” LED, which is on when all on-board supplies are normal;
- Amber “CX” LED driven by the CX3, slowly cycles on and off.
- Red “Err” LED, which is on for thermal overrun or other error states;

On Side 2, along the board edge:

- Green, Amber, and Red LEDs driven by [STM OR 24T6 OR CPLD] control bits.
- Amber LED driven by the FX3, slowly cycles on and off.

Table 1-12 AgatePXC/2 BIST Test Nodes

Access Method	Devices	Testing Method
I^2C	CY22393 Clk, 9DB403 Clk Bfr, ADV7441A Digitizer, 3x CPLD, LM75, LM63, 24LC256 EEPROM, ADS1015 4x ADC, MIPI Port, CX25858 EEPROM, FX3 and CX3 Controllers, 9X130 PCI/PCIe Bridge, 24T6 PCIe Switch, E4690 Graphics	Verify and Initialize Control Registers
UART	Debug access to the FX3 and CX3 Controllers	Examine and Verify
SWD	STM32F427	Debug Port
JTAG	3x CPLD, 9X130 PCI/PCIe Bridge, 24T6 PCIe Switch, CX3, FX3, E4690 Graphics	ID and Boundary Test
HSYNC, VSYNC	ADV7441A Digitizer, E4690 Graphics	STM Counters
Voltage	VDD_CORE, VDD_10, VDD_11, VDD_18, ancillary supplies	STM A/Ds + ADS1015
Temperature	STM on-chip sensor, LM63 and LM75 Thermal Sensors, E4690 Substrate Diode	poll via I^2C registers

1.14.6 LED Error Reporting (MerlinPXC)

On the MerlinPXC/2 front panel are:

- Green “St” LED driven by the STM, slowly cycles on and off.
- Green “V” LED, which is on when all on-board supplies are normal;
- Amber “C” LED driven by the CX3, slowly cycles on and off.
- Red “Er” LED, which is on for thermal overrun or other error states;

On Side 2, along the board edge:

- Green, Amber, and Red LEDs driven by [STM OR 24T6 OR CPLD] control bits.

Table 1-13 MerlinPXC/2 BIST Test Nodes

Access Method	Devices	Testing Method
I^2C	CY22393 Clk, 9DB403 Clk Bfr, 2x CPLD, LM75, LM63, 24LC256 EEPROM, ADS1015 4x ADC, MIPI Port, CX3 Controller, 9X130 PCI/PCIe Bridge, 24T6 PCIe Switch, E8860 Graphics	Verify and Initialize Control Registers
UART	Debug access to the CX3 Controller	Examine and Verify
SWD	STM32F427	Debug Port
JTAG	2x CPLD, 9X130 PCI/PCIe Bridge, 24T6 PCIe Switch, CX3, E8860 Graphics	ID and Boundary Test
HSYNC, VSYNC	E8860 Graphics (VGA)	STM Counters
Voltage	VDD_CORE, VDDCI, VDDR1, VDD_095, VDD_105, VDD_18, ancillary supplies	STM A/Ds + ADS1015
Temperature	STM on-chip sensor, LM63 and LM75 Thermal Sensors, E8860 Substrate Diode	poll via I^2C registers

1.14.7 LED Error Reporting (MerlinMTX)

On the MerlinMTX front panel are:

- Green “St” LED driven by the STM, slowly cycles on and off.
- Green “V” LED, which is on when all on-board supplies are normal;
- Red “Er” LED, which is on for thermal overrun or other error states;

On Side 2, along the board edge:

- Green, Amber, and Red LEDs driven by [STM OR 24T6] control bits.

Table 1-14 MerlinMTX BIST Test Nodes

Access Method	Devices	Testing Method
I^2C	CY22393 Clk, 9DB403 Clk Bfr, 1x CPLD, LM75, LM63, 24LC256 EEPROM, ADS1015 4x ADC, 9X130 PCI/PCIe Bridge, 24T6 PCIe Switch, E8860 Graphics	Verify and Initialize Control Registers
SWD	STM32F427	Debug Port
JTAG	1x CPLD, 24T6 PCIe Switch, E8860 Graphics	ID and Boundary Test
Voltage	VDD_CORE, VDDCI, VDDR1, VDD_095, VDD_105, VDD_18, ancillary supplies	STM A/Ds + ADS1015
Temperature	STM on-chip sensor, LM63 and LM75 Thermal Sensors, E8860 Substrate Diode	poll via I^2C registers

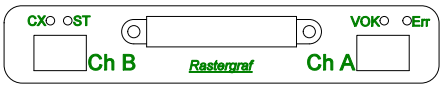
1.15 AgatePXC I/O Connectivity Options

The AgatePXC/2 includes the full feature set of the product line. The table on the following page provides details about the display capabilities of each model. Note that for Agate, you can have a total of 2 active displays at one time. The AgatePXC PIM adapter eases rear access connections.

AgatePXC/1x versions are available by special order.

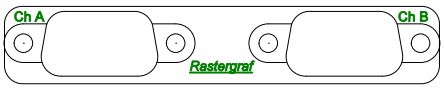
AgatePXC/2: Dual DisplayPort Outputs w/I/O

The AgatePXC/2 front panel connectors include 2 Mini DisplayPort (mDP) and a Honda SDR50 that supplies a multi-mode analog graphics output and audio and video inputs. VGA Ch A and B are available on the PMC Pn4 rear I/O.



AgatePXC/1V: Dual VGA Outputs

The AgatePXC/1V provides two front panel VGA connectors. Each channel supports RGBHV or RGB with composite or Sync-On-Green.



AgatePXC/1D: Dual DisplayPort Outputs

The AgatePXC/1D provides 2 Mini DisplayPort (mDP) connectors.

AgatePXC/1L: Single LVDS Output

The AgatePXC/1L provides a front panel Mini Camera Link pinout compatible Honda SDR26 connector.

AgatePXC/1R: Single VGA Output

The AgatePXC/1R provides one front panel VGA connector plus a Rastergraf RG-101 compatible VGA output on the PMC Pn4 rear I/O connector.

Table 1-15 AgatePXC Version Feature Summary

	Standard Version	Special Order Versions – contact Rastergraf			
	AgatePXC/2	AgatePXC/1R	AgatePXC/1V	AgatePXC/1D	AgatePXC/1L
AMD E4690 2D/3D w/512MB GDDR3	yes	yes	yes	yes	yes
XMC (x4/x8 PCIe 2.0)	yes	yes	yes	yes	yes
PMC 32/64 33-133 MHz 3.3 and 5V signaling	yes	yes	yes	yes	yes
Front Panel Access	SDR50+2x mDP	yes	2x VGA	2x mDP	1x SDR26
Rear Panel Access	PMC Pn4/, XMC Pn6	PMC Pn4, XMC Pn6	PMC Pn4	XMC Pn6	no
Dual DisplayPort	mDP, XMC Pn6	no	no	mDP, XMC Pn6	no
VGA Out Ch 1	PMC Pn4	no	VGA, PMC Pn4	no	no
VGA Out Ch 2 VGA/PAL/NTSC/HD	SDR50, PMC Pn4	PMC Pn4, XMC Pn6	VGA, PMC Pn4	no	no
Dual DVI Out	no	no	no	no	no
8 Ch NTSC/PAL In	SDR50, PMC Pn4, XMC Pn6	no	no	no	no
RGBHV In (using FX3 controller)	SDR50, PMC Pn4, XMC Pn6	no	no	no	no
DVI In	PMC Pn4, XMC Pn6	no	no	no	no
Audio In (stereo)	2x SDR50 2x PMC Pn4 or XMC Pn6	no	no	no	no
LVDS	no	no	no	no	1x SDR26
MIPI CSI-2 Input (using CX3 controller)	SDR50	no	no	no	no
USB2.0/3.0 port	XMC Pn6	no	no	no	no
Integrated System Monitor (ISM)	yes	yes	yes	yes	yes
CCPMC form factor compatible	yes	yes	yes	yes	yes
Conduction-cooled capable	no	no	no	no	no
Requires host 3.3V	yes	yes	yes	yes	yes
Field reprogrammable BIOS	yes	yes	yes	yes	yes
PIM Rear I/O Adapter	yes	yes	yes	yes	yes
Window and Linux	yes	yes	yes	yes	yes

1.16 MerlinPXC I/O Connectivity Options

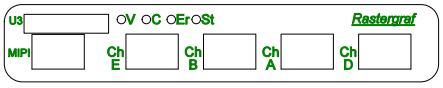
The MerlinPXC/2 includes the full feature set of the product line. The table on the following page provides details about the display capabilities of each model. Note that for MerlinPXC, you can have a total of 6 active displays at one time.

The MerlinPXC PIM adapter eases rear access connections.

MerlinPXC/1x versions are available by special order.

MerlinPXC/2: 6 DisplayPorts w/MIPI & USB

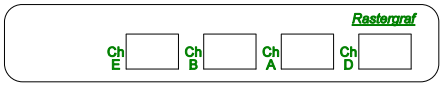
The MerlinPXC/2 front panel provides 4 Mini DisplayPort (mDP) connectors. In addition, it provides a MIPI CSI-2 1-4 lane camera input and a USB 3.0 port. 3 DisplayPort channels are available via the XMC or PMC rear I/O.



MerlinPXC/1D: 6 DisplayPort Outputs

The MerlinPXC/1D provides 4 Mini DisplayPort (mDP) connectors and 3 DisplayPort channels are available via the XMC or PMC rear I/O.

.



MerlinPXC/1V: Single VGA Analog Output

The MerlinPXC/1V provides one front panel VGA connector plus a PMC rear I/O connection that is RG-101 compatible.

Note that for multiple-channel VGA applications, you can use a MerlinPXC/1D with external mDP to VGA dongles.

Table 1-16 MerlinPXC Version Feature Summary

	Standard Version	Special Order Versions – contact Rastergraf	
	MerlinPXC/2	MerlinPXC/1V	MerlinPXC/1D
AMD E8860 2D/3D w/2GB GDDR5	yes	yes	yes
XMC (x4/x8 PCIe 2.0)	yes	yes	yes
PMC 32/64 33-133 MHz 3.3 and 5V signaling	yes	yes	yes
Front Panel Access	4x mDP 1xMIPI 1xMicro AB 3.0	1x VGA	4x mDP
Rear Panel Access	PMC Pn4, XMC Pn6	PMC Pn4	PMC Pn4
DisplayPort	4 mDP 3x on XMC Pn6 or PMC Pn4	no	4 mDP 3x on XMC Pn6 or PMC Pn4
VGA Out	PMC Pn4	VGA PMC Pn4	no
MIPI CSI-2 Input (using CX3 controller)	1xMIPI	no	no
USB2.0/3.0 port	1xMicro B 3.0 XMC Pn6 3.0 PMC Pn4 2.0	no	no
Integrated System Monitor (ISM)	yes	yes	yes
CCPMC form factor compatible	yes	yes	yes
Conduction-cooled capable	no	no	no
Requires host 3.3V	yes	yes	yes
Field reprogrammable BIOS	yes	yes	yes
PIM Rear I/O Adapter	yes	yes	yes
Window and Linux support	yes	yes	yes

1.17 MerlinMTX I/O Connectivity Options

The MerlinMTX is a special purpose version of the MerlinPXC. It is targeted towards applications requiring DVI on PMC Pn4 and includes VGA/PAL input support as well. USB and MIPI support as well as the PMC host bus interface are all deleted from the MerlinMTX.

Unlike any of the AgatePXC or MerlinPXC boards, under certain conditions, the MerlinMTX can be used in conduction-cooled systems. Please contact Rastergraf for more information.

Please not that Rastergraf does not intend to fully support the CC market. The MerlinMTX is a limited application board suitable for certain applications only.

The table on the following page provides details about the display capabilities of the MerlinMTX.

Although you might expect that because of the focus on PMC Pn4 rear I/O there would be a PIM, one is not available at this time due the limited, custom-application focus of the product.

MerlinMTX: 1 DP, 2 DVI, and Video In

The MerlinMTX has no front panel.

On PMC Pn4 is provided 1 DisplayPort and 2 single-link DVI ports. In addition, it provides a multi-channel NTSC/PAL with connections also on Pn4.

Table 1-17 MerlinPXC Version Feature Summary

	MerlinMTX
AMD E8860 2D/3D w/2GB GDDR5	yes
XMC (x4/x8 PCIe 2.0)	yes
PMC 32/64 33-133 MHz 3.3 and 5V signaling	no
Front Panel Access	no
Rear Panel Access	PMC Pn4 only
Graphics Outputs	1v DisplayPort 2x single-link DVI PMC Pn4 only
VGA Out	no
MIPI CSI-2 Input (using CX3 controller)	no
USB2.0/3.0 port	no
Integrated System Monitor (ISM)	yes
CCPMC form factor compatible	yes
Conduction-cooled capable	yes
Requires host 3.3V	yes
Field reprogrammable BIOS	yes
PIM Rear I/O Adapter	no
Window and Linux support	yes

1.18 Software Support

Rastergraf software support is available for Linux, VxWorks, and Windows. Please consult Rastergraf for specifics, as all packages are not available on all boards, systems, or OS versions.

From Rastergraf:

- Limited functionality SDL Graphics Subroutine Library for VxWorks and Linux (Agate only)
- VGA BIOS for E4690 and E8860
- BIOS, drivers, and demo program for CX25858 digitizer
- BIOS and drivers for uPD720201 USB host controller
- Firmware for STM32F427 and ADV7441A
- Demo software for CX3 and FX3 to support selected cameras.

From other suppliers

- VxWorks OpenGL for E4690: c3itop and coreavi
- VxWorks OpenGL for E8860: c3itop and coreavi
- Windows and Linux Drivers for E4690 and E8860: AMD
- SDKs for the FX3 and CX3 are available from Cypress

IPMI software sources for programming XMC PROM – as yet unverified

https://www.supermicro.com/solutions/SMS_IPMI.cfm

http://sourceforge.net/projects/ipmiutil/

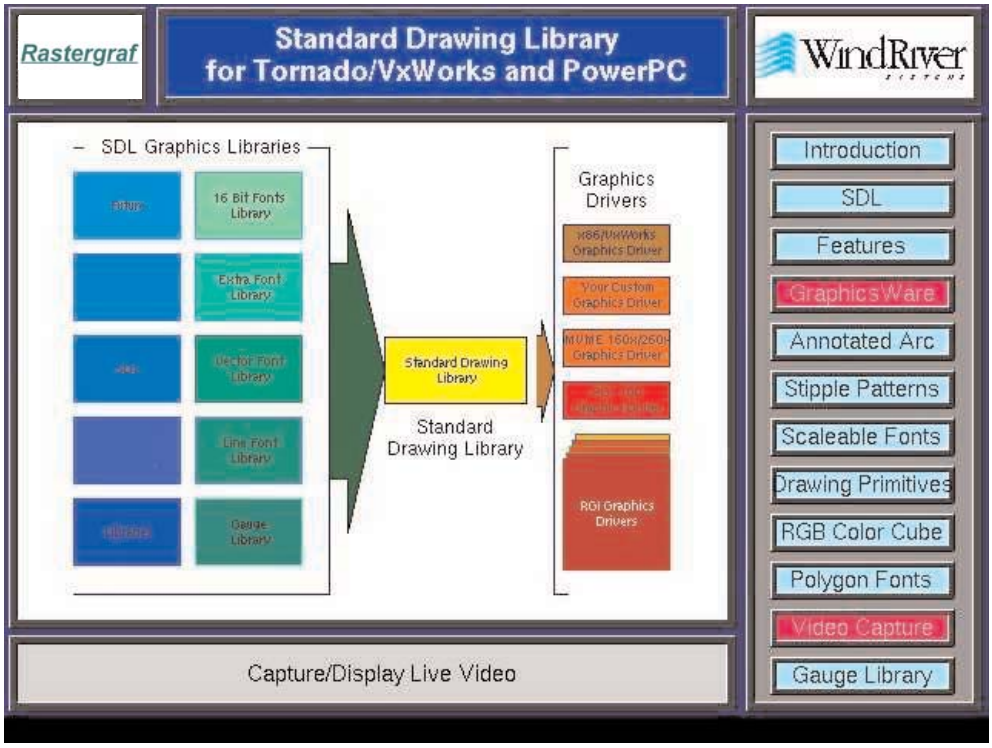
http://ipmiutil.sourceforge.net/

http://www.gnu.org/software/freeipmi/

https://msdn.microsoft.com/en-us/library/aa391402(v=vs.85).aspx

https://www.opalkelly.com/tools/fmceepromgenerator/

1.19 SDL: Standard Drawing Library (Agate Only)



SDL is a traditional 2D graphics library designed to be a device-independent programming interface. In this way, it is possible to upgrade from an earlier SDL-supported Peritek, Curtiss-Wright, or Rastergraf graphics board to an Agate without having to start from scratch.

Rastergraf provides only limited* SDL *support for Agate and none at all for Merlin due to the unavailability (from AMD) of crucial programming data for the graphics chips.

SDL is ideally suited to demanding board level and embedded systems applications. Drivers are available for selected host CPU boards running under DOS, Linux, or VxWorks. It is required that the OS/CPU combination be supported by the GNU C compiler and linker. SDL is not available in source.

SDL is supplied in object library format. It includes a set of “dumb frame buffer” graphics primitives. All graphics primitives are drawn as single pixel lines. Rectangles, polygons, circles, ellipses, and chords can be filled with a solid color or stipple patterns. More information about SDL is contained in the ***Standard Drawing Library C Reference Manual*** that is available for download from rastergraf.com.

SDL Feature Summary

- Solid (thin and wide) and dashed lines, polylines, and rectangles
- Pixblits to/from the display and host memory
- Filled and hollow polygons, ellipses, circles, sectors, and chords
- Solid and Pattern Fills – Pixel Processing
- Proportional and Fixed Width Fonts
- Clipping Rectangle and Logical Origin
- Support for DOS, Linux, and VxWorks
- Software Compatible with earlier SDL-supported graphics boards (except video input and STANAG)

Table 1-18 SDL Hardware Function Support

Feature	Agate Channels
DisplayPort: 640x480 to 2560x1600	2
LVDS: 2048x1536 (Agate)	1
VGA: 640x480 to 2048x1536	2
Sync On Green	yes
8/16/24 bpp	yes
NTSC/PAL	no
Video In	no

1.20 Other Rastergraf Products

For more information about our products, please consult our web page at http://www.rastergraf.com

1.20.1 Eclipse3PMC

Features a Borealis 2D/3D 128-bit graphics accelerators, UVGA resolution, OpenGL pipeline, and 16 or 32 MB SGRAM, analog RGB ***and/or*** DVI output with a 33/66 MHz, 32-bit PMC host interface.

Drivers are available for Windows XP/7, Linux, Solaris, and VxWorks.

1.20.2 GeminiPMC

Features two Borealis 2D/3D 128-bit graphics accelerators, UVGA resolution, OpenGL pipeline, and 16 MB SGRAM/channel with a 33/66 MHz, 32-bit PMC host interface. The /V version supports 2 VGA channels. The /D version provides a 68-pin connector and requires breakout cable for 2x VGA or DVI outputs.

Drivers are available for Windows XP/7, Linux, Solaris, and VxWorks.

1.20.3 TopazPMC

The TopazPMC features a 2D 64-bit graphics accelerator and 16MB SDRAM with a 33/66 MHz, 32-bit PMC host interface. Provides up to two independent, active VGA graphics channels. Other versions include a single/dual display LVDS or a single DVI channel plus single VGA channel. Other features include a BT835 PAL/NTSC decoder and AD9882 RGB/DVI decoder.

The TopazPMC/1S is a single display-only version that supports accurate STANAG 3350 A, B, and C timing modes.

Drivers are available for Linux and VxWorks. Due to legacy BIOS issues, the Topaz is not recommended for Windows.

1.20.5 Carrier Boards

PMA-P Single PMC to short PCI passive (bridgeless) adapter board;

PMB-P Single PMC to short PCI active (bridged) adapter board;

PMA-C Single PMC to 3U CPCI passive (bridgeless) adapter board;

PMX-P Single XMC to PCI adapter board with PIM I/O.

PME-P Single PCIe to PCI adapter board.

PMF-E Single XMC/PMC to PCIe adapter board.

1.21 References

Rastergraf provides documentation includes the board's User Manual and Standard Drawing Library (SDL) Manual.

You can obtain some technical literature from the links shown below. As you will see, some vendors require a Non-Disclosure Agreement (NDA) to gain access to information they consider proprietary. Given the trouble it is the NDA processed, you should know that in the case of AMD, Conexant, and Renesas, the information provided under NDA is not enough by itself to understand how to program the respective chip.

Note that since web links change, if any of the links provided are broken, just go the manufacturer's main web page and look for the part number.

AMD E4690 Embedded Graphics Controller

User Manual and Register Manual available from AMD under NDA

E4690 Data Brief

AMD E8860 Embedded Graphics Controller

User Manual and Register Manual available from AMD under NDA

E8860 Data Brief

ADV7441A RGB/DVI Decoder Data Sheet

ADV7441A Data Sheet

Conexant CX25858 8-Channel Audio/Video Decoder Product Brief

User and Programming Manuals available from Conexant under NDA

CX25858 Data Brief

IDT 89HPES24T6G2 24-Lane PCIe 2.0 Switch

89HPES24T6G2 Data Sheet

Renesas uPD720201 USB 2.0/3.0 Host Controller Data Brief

User and Programming Manuals available from Renesas under NDA

uPD720201 Data Brief

Pericom PI7C9X130 PCIe to PCI Bridge Data Sheet

PI7C9X130 Data Sheet

Cypress CX3 and FX3 Data Sheets

CX3 Data Sheet
FX3 Data Sheet

ST Micro STM32F427 Data Sheet

STM32F427 Data Sheet

FlatLink Data Transmission System, Design Overview (LVDS)

Flatlink Data Transmission System Design Overview

SMPTE-170M

Composite Analog Video Signal – NTSC 2004 edition

SMPTE 170M-2004

ITU-R BT.470

Conventional Television Systems, Revision 7

ITU-R BT.470

DisplayPort

VESA controls access to the DisplayPort documentation. You can still get version 1.1a freely, but subsequent versions must be purchased. It's cheaper to join VESA ($3.5K for small companies) than to pay the non-member prices for documentation. Here is a link to VESA membership.

PCI Express and PCI

PCISIG controls all PCI related documentation. It's cheaper to join PCISIG ($3K) than to pay the non-member prices for documentation. Here is a link to PCISIG membership.

PMC and XMC

The PMC and XMC standards are administered by VITA. It's cheaper to join VITA for a quarter-year ($750) than to pay the non-member prices for documentation. Here is a link to VITA membership.

Graphics Textbooks

Fundamentals of Interactive Computer Graphics

Addison Wesley, 1993. Foley and Van Dam

Principles of Interactive Computer Graphics

McGraw-Hill, 1979 Newman and Sproull

Manual Style Guide and Computer Lingo Abbreviations

IEEE Computer Society Style Guide

1.22 Common Analog Video Formats

RS-170

RS-170 is defined as 525 lines by 30 frames/second and is the standard black and white video format used in the North America, Japan, and a few other parts of the world. RS-170 specifies a 15.75-KHz horizontal and a 60-Hz vertical interlaced scan frequency (refresh rate) as well as other aspects of the composite signal such as voltage, sync levels and timing of sync and blanking. The 60 Hz refresh rate was used to avoid picture artifacts from induced (60 Hz) power line fields.

Interlace

At the time that RS-170 was developed, electronic systems were not fast enough to permit all 525 lines to be drawn in the $1/60^{th}$ of a second that is the basis of the timing specification. A technique called interlace was developed to allow the entire screen to be drawn at $1/30^{th}$ of a second and to do it in a way that would minimize the picture degradation apparent at 30 Hz. Interlace draws half the lines each $1/60^{th}$ of a second. The first pass (or field) draws all the odd lines. The second pass draws all the even lines. Thus, in $1/30^{th}$ of a second the entire image has been drawn. Interlace masks the fading of the phosphors and changes the gradual fading top to bottom and a change in brightness to the illusion of flicker, or jumping when you look closely.

Basic RS-170 Video Signal

The video signal encodes light intensity as a function of voltage. Position is represented by time and is relative to horizontal and vertical synchronization information. Sync information is added into the basic video signal below the blanking level.

RS-170 was the original "black-and-white" television signal definition, per EIA. It defined a 75Ω impedance system and a 1.4V (peak-to-peak, including sync) composite (video and sync) signal:

```
White:  +1.000V
Black:  +0.075V
Blank:  (0V reference)
Sync:   -0.400V
```

Although RS-170 is still a commonly used reference signal, its nominal signal peak-to-peak level has been modified to 1.0V (peak to peak) by a borrowing from the RS-343 standard (see below).

RS-170 RGB

Refers to Red, Green, and Blue (TGB) signals timed to RS-170 specifications. Since the RGB signals are actually individual monochrome

signals representing their respective colors, RS-170 RGB merely refers to three black and white signals sharing one sync signal.

The sync can be provided in 3 ways:

a) Sync-on-Green adds in a negative going .3V composite sync level into the .7V Green signal and is basically the same as RS-170.

b) Separate composite sync. This is a TTL level signal that includes both horizontal and vertical sync. It is known as RGBS.

c) Separate sync. TTL level horizontal and vertical sync signals are supplied for a 5 wire system (RGBHV).

Digitizing RS-170 video

A typical digital image produced by video digitization would have a resolution of 512 (horizontal) x 480 (vertical) pixel resolution and would have individual pixels with a 5:6 aspect ratio. Square pixels can simplify image spatial analysis and editing operations: a common square pixel format is 480 lines at 640 pixels per line.

RS-170A

RS-170A was derived from RS-170 for the purpose of including color information, still contained in a single channel, and is used for television in the United States and Japan. RS-17A video incorporates a "subcarrier" for encoding color; color information is phase encoded by a lower frequency chrominance signal superimposed on the luminance signal, and is compatible with systems that only work with the original B&W RS-170.

Related NTSC-derived video formats

Monochrome NTSC

Color NTSC video format RS-170A has evolved from RS-170 standard and is nowadays more often seen term than RS-170. Sometimes term "monochrome NTSC" when referring to the old RS-170 specification.

S-Video

The two-signal (or wire) version is known as "S-video". The Y channel carries combined intensity and timing signals consistent with RS-170 mono. The C channel carries a separate color signal. S-video is usually two coax cables in a single bundled cable with 4-pin mini-DIN connectors.

RS-330

RS-330 is used by closed-circuit TV and studio cameras. It similar to RS-170, but H-sync pulses are absent during V-sync. Equalizing pulses are not required and may be added optionally during the V-blanking interval.

RS-343A

RS-343A was introduced as a signal standard for "high-definition closed-circuit television", which among other things reduced the total signal amplitude to 1.00Vp-p. The signal specifications according RS-343A:

```
White: +0.714V
Black: +0.054V
Blank: (0V reference)
Sync: -0.286V
```

RS-343A specifies a 30 Hz interlaced scan with a composite sync signal with timings that produce a scan at 675 to 1023 lines.

This standard is typically used by high resolution video cameras, precision imaging systems, infrared targeting, low-light TV, night-vision and special military display systems.

CCIR

The CCIR is a standards body that defined the 625 line 25 frames/second interlaced TV standard used in many parts of the world. The CCIR standard defines only the monochrome picture component, and there are two major color encoding techniques used with it, PAL and SECAM.

```
Line period         64us (Micro-seconds)
Line blanking       12.05 +/- 0.25us
Line sync           4.7 +/- 0.1us
Front porch:        1.65 +/- 0.1us
```

For the PAL format the following extra details were defined:

```
Color burst start   5.6 +/- 0.1us after sync start.
Color burst         10 +/- 1 cycles
Color subcarrier    4.433 MHz
```

VGA

There never really WAS an official standard for VGA video, but it is very close to the RS-343 signal standards and has myriad of timing formats.

STANAG 3350 A

Follows RS-343A.

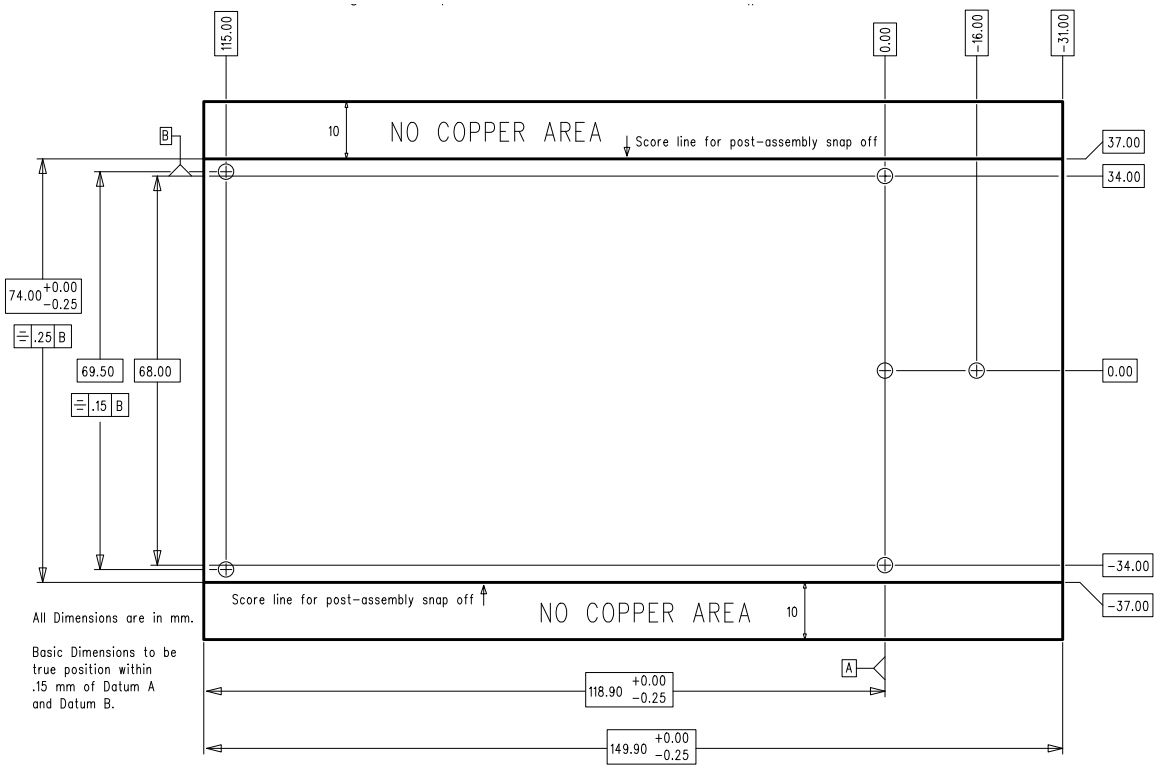
STANAG 3350 B

Follows CCIR 472-1 (PAL).

STANAG 3350 C

Follows RS-170 (NTSC). Essentially RS-170 RGB

Chapter 2
Specifications



2.1 Certifications and Statements

CAGE:	Commercial and Government Entity (CAGE)	3HXC2
DUNS:	Data Universal Number System (DUNS)	136771743
FSC:	Federal Supply Class (FSC)	5998
NAICS:	North America Industry Classification System (NAICS)	334119
SIC:	Standard Industrial Classification (SIC)	3577

RoHS: Rastergraf boards are built to RoHS lead-free standards.

In addition, in the interest of equipment and customer safety, Rastergraf does not use any tantalum-based capacitors.

What is the safety issue? Automated equipment may sometimes install a capacitor backwards, which for tantalum capacitors is reverse polarized. This can lead to an overheated device and, over time, cause serious damage to the PCB and even cause the component to explode.

REACH: No hazardous chemicals are included as part of these products.

ISO and IPC: Rastergraf products are built by Contract Electronics Manufacturers (CEM) who are IPC Class III Compliant, RoHS Compliant, ISO 9001:2000 Certified, and IPC-610 trained. Please contact Rastergraf for more information.

UL: Rastergraf uses UL certified FR4 PCB material.

Conflict Minerals: Defined as the use of specific minerals (tantalum, tin, tungsten and gold) originating in the Democratic Republic of the Congo (DRC) or surrounding countries.

While as a small, privately-held company, Rastergraf is not required to comply with the related Sarbanes-Oxley regulation, Rastergraf request that its suppliers do comply.

Rastergraf is unable to provide smelter-level full traceability for each component used in its products. That said, Rastergraf can provide under NDA a list of the manufacturers of its components.

2.2 General Features

Data Security: Note that it isn't possible for any Agate or Merlin on-board device to save image data from on-board graphics memory. Also, when power is removed, all image data stored in the graphics memory disappears.

Host Bus Interface: Both the AgatePXC and MerlinPXC provide a dual bus interface, supporting both the newer serial bus PCI Express (PCIe) on XMC connector Pn5, and the older parallel data PCI bus on PMC connectors Pn1, Pn2, and Pn3.

The MerlinMTX supports ONLY the XMC link.

PCIe Bus Usage: x4 or x8 lanes, PCIe 1.1 (2.5Gb/s) or PCIe 2.0 (5.0 Gb/s).

**** PMC (PCI) Bus Usage:*** 32/64-bit, 33/66/100/133 MHz, Pn1- Pn3, PCI/PCI-X

The low 4 lanes of the on-board PCIe are shared via multiplexers with a PCI7C9X130 PCIe to PCI bridge which supports PCI/PCI-X up to 133Mz on the PMC connectors.

Operation on a passive PMC-PCI carrier board at 66 MHz or above may be unreliable. It is recommended that you use an active version that has a local PCI-PCI bridge.

**** PCI bus Interrupts:*** The 9X130 can interrupt the PCI bus on the INTA-D lines.

**** PCI Bus Master:*** The 9X130 can assume bus mastership of the PCI.

**** PCI Bus Loading:*** One PCI 2.1 compatible load

**** AgatePXC and MerlinPXC only***

PMC Compatibility: Complies with IEEE 1386-2001 except:

PMC Side 2 Clearance The Agate and Merlin both violate the PMC Side 2 component height specification. This is not a big deal. Only ***non-conductive*** component elements are involved.

Background: the interboard separation plane dimension defines the dividing line between two host boards in an IEEE 1101 type chassis. This dimension is 16.26 mm above the plane of the host board and must be observed.

The standard PMC Side 2 height limit = [3.5 mm - PCB thickness]. The nominal PCB thickness is 1.6 mm, so the standard height limit would be 1.9 mm. However,

16.26 mm	host side 1 surface to interboard separation
- 10 mm	PMC standoff
- 1.6 mm	Agate or Merlin **nominal** PCB thickness
= 4.66 mm	net maximum distance to separation plane.

We have chosen to use 4.0 mm as specification "override" for ***non-conductive*** components.

We have not encountered any significant customer problems with this expanded limit in more than 20 years and several generations of boards.

CCPMC Compatibility: The AgatePXC and MerlinPXC board layouts follow VITA 20 CCPMC in many respects in order to make the boards more compatible in a wider range of applications. Even so, ***the boards are NOT INTENDED FOR USE IN TRUE CCPMC APPLICATIONS.***.

However, the MerlinMTX is designed for CCPMC use and closely follows VITA 20. Thus, no front panel connections or even a front panel is included with the board. I/O connections are made through the PMC Pn4 connector.

Crucial MerlinMTX Note: Sections of the gold plated areas on Side 1 are connected either to circuit ground or VDD_10.

YOU MUST ISOLATE the gold-plated areas on Side 1 of the board when installing any heat sink or other thermal interface. Use thermal gaskets as covered in the Curtiss-Wright PMC/XMC Installation Guides.

XMC Compatibility: Follows VITA 42.0 and VITA 42.3. Note that XMC depends on IEEE 1386 for mechanical specifications.

A case could be made for offering VITA 60 connectors in place of the standard Samtec VITA 42.3 connectors, since the VITA 42.3 connectors are not technically qualified for 5.0 Gb/s operation that PCIe 2.0 requires. That said, lots of products do run with these connectors at PCIe 2.0 speeds.

If VITA 60 connectors are of interest, please contact Rastergraf to discuss it. There is no reason why an Agate or Merlin could not be built with them.

Module Size: IEEE 1386-2001 compatible, 149 mm x 74 mm

Environment:

Humidity:	5% to 90%, non-condensing
Temperature:	-55 to +85 degrees C, storage
Temperature:	0° to 65° C, operating

Front and Rear Access: The AgatePXC and MerlinPXC provide access to most I/O features on both front panel and Pn4/Pn6 rear I/O connectors. Please refer to Tables 1-11 and 1-12 for details.

The AgatePXC or MerlinPXC can be supplied with no front panel connectors. In this case, only the connector grounds are still connected to circuit ground. All other connections are open.

As noted above, the MerlinMTX requires that all I/O connections be made through the PMC Pn4 rear I/O connector.

Rear I/O Compatibility: Follows VITA 46.9. For full feature access, requires:

P64s (AKA P32d) for full PMC Pn4 connectivity

X8d+X12d+X38s for full XMC connectivity. Subsets can be accommodated at the cost of reduced functionality. Chapter 4 covers all of this in excruciating detail.

Many of the rear I/O signals are high speed differential pairs which require matched length pairs and 100Ω impedance. Many older carrier and CPU boards were not designed with this in mind and will therefore likely not be suitable. Please investigate thoroughly before committing to a rear panel access system design.

Rear Transition Modules: Otherwise known as RTMs, these are half-size cards that plug into the back of the system backplane and bring out the host board's rear I/O signal set to standard connectors.

An RTM may include a position for a VITA 36 PMC I/O Module (PIM). A PIM provides connectors for a specific set of I/Os on a matching PMC or XMC board which can greatly aid in the rear panel system integration effort.

Rastergraf provides PIMs (see Chapter 4) for all Agate and Merlin boards.

Power Requirements: All versions of ***REQUIRE+3.3V and +5V (or +12)***

Please see Section 2.3, 2.4, and 2.5 for board specific power requirements.

I/O Connector Power: The Agate and Merlin supply fused +3.3 and +5V to many of the I/O interface connectors.

Remember when calculating the overall board power consumption that I/O connector power can add up.

Each connector is independently protected by a Positive Temperature Coefficient (PTC) resistor. It resets automatically when an overload is removed.

Please note that the power rating is nominal and it is possible to exceed this rating by a significant amount, at least in the short term. The part used in all cases is the Bourns MF-FSMF050X-2, rated 0.5A hold.

DisplayPort: each channel, 3.3V@0.5A PTC "fuse";

VGA or DVI: each channel, 5V@0.5A PTC "fuse";

P4 F5V:	5V@0.5A PTC “fuse”;
P6 F5V:	5V@0.5A PTC “fuse”;
STM SWD:	3.3V@0.5A PTC “fuse”;
USB:	5V@0.5A nom, 1.3A trip, controlled by TPS2015B;
MIPI:	3.3V@0.5A, nom, 1.3A trip, controlled by TPS2015B; V optionally 5V or 1.8V.

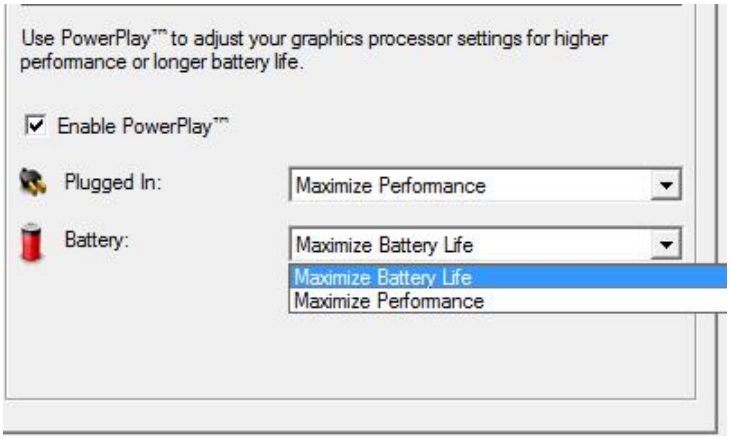
Power Saving Features

There are two proactive ways you can affect the power consumption of the Agate or Merlin:

PCIe Bus Speed:

As implemented on both boards, the PCIe is driven by the 89HPES24T6G2 PCIe switch which passes the PCIe streams between the local devices and the host CPU. The PCIe bus speeds of the local devices ***except the GPU*** are auto-negotiated by the 24T6 and not readily changed.

The host system controls bus speed of both the host side of the 24T6 and the 24T6’s GPU local port(s) using the AMD Catalyst Control Panel/Advanced/PowerPlay. Enable PowerPlay and choose between Maximize Battery Life and Maximize Performance. Battery selects PCIe 1.1 (2.5Gb/s transfer rate) and Performance selects PCIe 2.0 (5.0Gb/s transfer rate.



Unless you are doing a lot image manipulation and transfers between host and board, you are unlikely to see any difference moving to PCIe 2.0 (5.0Gb/s), whereas the power dissipation on the board increases by several watts.

PCIe Lane Width: DIP switches on the Agate or Merlin independently select bus width for x4 or x8 for the host and for the GPU lanes. Again, unless you are do a lot with the board, x4 will usually be more than adequate and again, you can reduce power dissipation by a few watts.

Cooling Considerations:

IMPORTANT: GOOD AIRFLOW IS REQUIRED.

You should be able to measure at least 400 Linear Feet per Minute (LFM) at the board if you want to operate at the upper temperature limits. You can usually get this much air by using a 100 CFM-rated fan.

Due to the high component density and functionality of the Agate and Merlin boards, the power consumption seriously exceeds the nominal PMC 7.5W specification. Many PMC products do this, but it is still necessary to be careful about it. We have seen problems when:

a) the carrier board current limits the power supplied to the PMC slot. For adequate margins, you need at least 15W each for 3.3V and 5V (or 12V).

b) the board is mounted on a carrier, used in a PC, and there is no fan. Please use a carrier with a built-in fan or rig up an external fan that funnels air onto the graphics board. Without a fan, the Agate or Merlin will quickly overheat.

Ruggedization Option: Rastergraf is not in the militarized business, but it can supply boards in a semi-ruggedized form, with conformal coating and extended temperature testing.

As compared to the fully ruggedized products supplied by such companies as CW Defense or GE Automation which use mil-grade components and provide full component level traceability, Rastergraf board designs use standard distribution grade ***commercial temperature range or industrial temperature range components. Also, no formal component tracking system is maintained.***

The board is protected with a conformal coating. It is Miller Stephenson MS-460A spray-on, and is MIL-I-46058C, Type SR and MIL-T-152B compliant. The board is tested under extended temperature conditions:

Temperature: -40 to +71º C, operating
-55 to +125º C, storage

Ruggedization Levels: The following table shows the standard ruggedization levels. At the time of writing, complete shock and vibration testing has not been performed, but some boards have been tested enough to expect full acceptance is possible. Please contact Rastergraf Sales if you need this information.

Table 2-1 Rastergraf Ruggedization Levels Chart

Spec	Air-Cooled Level 0	Air-Cooled Level 50	Air-Cooled Level 100	Air-Cooled Level 200	Conduction-cooled Level 100
Applicable Graphics Board(s)	Argus Gemini Eclipse3 Topaz Merlin Agate	Gemini Eclipse3 Topaz Merlin Agate	Gemini Eclipse3 Topaz Merlin Agate	Eclipse3 Topaz	MerlinMTX
Operating Temperature (4, 6)	0°C to 50°C	-20°C to 65°C	-40°C to 71°C	-40°C to 85°C	-40°C to 71°C
Storage	-40°C to 85°C	-40°C to 85°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C
Humidity Operating	0 to 95% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing
Humidity Storage	0 to 95% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing
Vibration Sine (1)	2 g peak 15-2 kHz	2 g peak 15-2 kHz	10 g peak 15-2 kHz	10 g peak 15-2 kHz	10 g peak 15-2 kHz
Vibration Random (2)	0.01 g2/Hz 15-2 kHz	0.02 g2/Hz 15-2 kHz	0.04 g2/Hz 15-2 kHz	0.04 g2/Hz 15-2 kHz	0.1 g2/Hz 15-2 kHz
Shock (3)	20 g peak	20 g peak	30 g peak	30 g peak	40 g peak
Conformal Coat (5)	optional	optional	optional	optional	yes
Order Option (7)	/CA or /CS	/A5A or /A5S	/A1A or /A1S	/A2A or /A2S	/C1A or /C1S

Notes:

1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15 to 44 Hz, depending on specific test equipment. Shock and Vibration values not completely verified.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow. Consult the factory for details.
5. Conformal coating type to be specified by customer. Consult the factory for details.
6. Temperature is measured at the card interior (not at edge).
7. Last letter in ordering option: A for Acrylic Conformal Coating, S for Silicone Conformal Coating

ESD Protection:

Agate and Merlin PMC, XMC, and PIM I/O paths are protected by ESD TVS. Several devices are used according to routing and placement requirements:

1) Littelfuse SP3003-04XTG: Quad ESD TVS protection diodes for single-ended signals
2) Semtech RCLAMP0524PATCT: Quad ESD TVS protection diodes for high-speed differential signals
3) Semtech RCLAMP0522T.TCT Dual ESD TVS protection diodes for high-speed differential signals

Table 2-2 ESD Protection Coverage

Signal Name	Signal Type	Applicable Board(s)	Comments
DVxy	DVI Differential Pairs	MerlinMTX, MerlinPXC PIM	
DVx_HPD, DPx_AUXn	DVI Control Signals	(as above)	
DPxy	DisplayPort Differential Pairs	AgatePXC, AgatePXC PIM MerlinPXC, MerlinPXC PIM	
DPx_HPD, DPx_PIN13, DPx_AUXn	DisplayPort Control Signals	(as above)	
USB_RX, TX, D	USB Differential Pairs	(as above)	
VGA: RGBHV, DDCxx	VGA signals	(as above)	
DV PWR, DP PWR, VGA PWR, USB PWR, MIPI PWR	External Device Power	As appropriate	NO ESD by design
MIPI_D, CK, SCL, SDA	MIPI Differential Pairs and I^2C	AgatePXC, MerlinPXC	
STM USB Dn (side connector)	STM USB Differential Pair	AgatePXC, all Merlin	
PDW_Dn	WandCam Differential Pairs	AgatePXC PIM, MerlinPXC PIM	
PDW_DVPDx, CTL	YUV Camera Signals	AgatePXC PIM	
LVDS_Un, Ln	LVDS Differential Pairs	AgatePXC/1L	
VINx, AINx	CX25858 A and V Inputs	AgatePXC/2, MerlinMTX	
DVI_INx	DVI Input Differential Pairs	AgatePXC/2	
RGBHV_In	RGBHV Input Signals	AgatePXC/2	
Rear RG-101 MUX (Section 4.9.4)	VGA Output	AgatePXC	
Rear RG-101 MUX (Section 4.9.4)	VGA Output	MerlinPXC	Omitted *
CX3 UART RX, TX (optional header)	CX3 Debugger Port	AgatePXC, MerlinPXC	Omitted *
FX3 UART RX, TX (optional header)	FX3 Debugger Port	AgatePXC	Omitted *
GP I^2C (optional header)	I^2C control	All	Omitted *

* Since these are not often used, it is not a serious issue

2.3 Specifications Unique to AgatePXC

Agate Graphics Processor: AMD E4690 Multi-Chip Module (MCM).

(AKA M96 CSP or RV730, PCI Dev ID 9491)

See Sections 1.2 and 1.4 for detailed information about the E4690.

Maximum VGA Dot Clock 400 MHz

Horizontal Scan Rates 31.5 to 115 KHz

Display Memory: 512MB GDDR3 on-chip memory.

Display Colors 16.7 Million @ 24-bits

BIOS PROM: 128KB Flash EEPROM contains the VGA BIOS. Second EEPROM can be installed for customer use (special order).

Graphics Outputs: ***Only 2 channels can be active at any time***

Digital: /1D or /2 version:
2x DisplayPort on front panel (Channels A and B)
2x DisplayPort on XMC Pn6 (Channels C and D)

/1L version:
1x LVDS - on front panel
single link (single pixel/clock) or
dual link (two pixels/clock)

Analog: /1V or /1R version:

2x VGA on front panel (Channels A and B)
2x VGA on PMC Pn4 (same Ch A and B)

Composite Video Signal: A multiplexer selects Sync-On-Green operation. The signal has the following approximate values:

1 Volt peak to peak consisting of:
660 mV Reference White +
54 mV Reference Black +
286 mV Sync Level

PMC/PCI Bus Interface **Pericom PI7C9X130** 32/64-bit, 33-133 MHz PCI/PCI-X to PCIe 1.1 x4 Bridge. Supports Universal PCI Bus signaling (5V and 3.3V) on the PMC side.

XMC/PCIe Bus Interface **IDT 89HPES24T6G2** 6 port PCIe 1.1/2.0 PCIe switch; each port is x4 PCIe lanes.

Ports 0&1: XMC: x4 or x8, PCIe 2.0;
power save options: x4 only, PCIe 1.1;

Port 0: PMC: x4 to Pericom PCIe to PCI bridge, x4, PCIe 1.1. x4 Port 1 not used.

Ports 2&3: connected to E4690, x4 or x8, PCIe 2.0; power save options: x4 only, PCIe 1.1;

Port 4: connected to uPD720201, x1, PCIe 2.0;

Port 5: connected to CX25858, x1, PCIe 1.1

USB Host Controller **Renesas uPD720201**, PCIe 2.0 PCIe, four port, USB 3.0/2.0 compliant, switched power control. BIOS PROM.

Port 1 to STM32F427 BIST controller;

Port 2 to Cypress CX3 MIPI CSI-2 camera controller;

Port 3 to user XMC rear I/O;

Port 4 to Cypress FX3 Peripheral Controller.

Video/Audio Digitizer **Conexant CX25858**, 8 NTSC/PAL Composite Video In, 8 Audio In (standard Agate connects 2), all channels can be active at once. Video capture mode is 4:2:2 or 4:1:1, choice of NTSC or PAL affects all inputs; pairs of audio inputs can be configured for stereo. 2Kb Serial EEPROM stores power-up configuration. BIOS PROM.

RGBHV/DVI/YUV Digitizer **Analog Devices ADV7441A** captures RGBHV (SOG or separate sync) or DVI up to 1600x1200x16bpp; interfaces to **Cypress FX3** USB 3.0 Peripheral Controller and uses modified Cypress video input application software. Front panel supports RGBHV in only. Rear I/O supports RGBHV or DVI.

The ADV7441A output can be disabled and an 8-bit YUV camera can be connected via a mid-board connector to drive the FX3.

MIPI CSI-2 Digitizer **Cypress CX3** USB 3.0 controller for MIPI CSI-2 1-4 lanes captures high resolution camera input.

Power Requirements AgatePXC easily exceeds the nominal power limits of PMC (7.5W). XMC is controlled by the amount of available cooling and host power supply capabilities. In order to achieve full operability, the AgatePXC/2 requires:

Host Bus	Voltage Input	Idle*	Full Operation*
PMC/XMC	3.3V	0.5A	2A
PMC	5V	1.75A	6.85A
XMC	VPWR=5V	1.75A	6.85A
	VPWR=12V	1.1A	3A

**** Doesn't include power drawn through I/O connectors.***

Power-management: With the proper software, the graphics controller can power-down unused functions.

Front Panel I/O Connectors	AgatePXC/1V:	Dual VGA
	AgatePXC/1D:	Dual Mini DisplayPort (mDP)
	AgatePXC/1L:	Honda SDR26
	AgatePXC/1R:	Single VGA
	AgatePXC/2:	2x mDP + Honda SDR50
Rear I/O Connectors	AgatePXC/1V:	PMC Pn4, XMC Pn6
	AgatePXC/1D:	PMC Pn4, XMC Pn6
	AgatePXC/1L:	PMC Pn4, XMC Pn6
	AgatePXC/1R:	PMC Pn4, XMC Pn6
	AgatePXC/2:	PMC Pn4, XMC Pn6

2.4 Specifications Unique to MerlinPXC

Merlin Graphics Processor: AMD E8860 Multi-Chip Module (MCM).

See Sections 1.3 and 1.4 for detailed information about the E8860.

Display Memory: 2GB GDDR5 on-chip memory.

BIOS PROM: 128KB Flash EEPROM contains the VGA BIOS. Second EEPROM can be installed for customer use (special order).

Graphics Outputs: ***6 channels can be active at any time***

Digital: /1D or /2 version:

4x DisplayPort on front panel (Channels A, B, D, E)

High speed multiplexer shares Channel D between front and rear.

/2 version:

3x DisplayPort on XMC Pn6 (Channel C, D, F)
3x DisplayPort on PMC Pn4 (Channel C, D, F)

High speed multiplexer shares Channel C, D, F between PMC Pn4 and XMC Pn6.

Analog: /1V version:

1x VGA on front panel
1x VGA on PMC Pn4 (if installed)

Composite Video Signal: The signal has the following approximate values:

1 Volt peak to peak consisting of:
660 mV Reference White +
54 mV Reference Black +
286 mV Sync Level

PMC/PCI Bus Interface **Pericom PI7C9X130** 32/64-bit, 33-133 MHz PCI/PCI-X to PCIe 1.1 x4 Bridge. Supports Universal PCI Bus signaling (5V and 3.3V) on the PMC side.

XMC/PCIe Bus Interface **IDT 89HPES24T6G2** 6 port PCIe 1.1/2.0 PCIe switch; each port is x4 PCIe lanes.

Ports 0&1: XMC: x4 or x8, PCIe 2.0;
power save options: x4 only, PCIe 1.1;

Port 0: PMC: x4 to Pericom PCIe to PCI bridge, x4, PCIe 1.1. x4 Port 1 not used.

Ports 2&3: connected to E8860, x4 or x8, PCIe 2.0;
power save options: x4 only, PCIe 1.1;

Port 4: connected to uPD720201, x1, PCIe 2.0;

Port 5: not used.

USB Host Controller **Renesas uPD720201**, PCIe 2.0 PCIe, four port, USB 3.0/2.0 compliant, switched power control. BIOS PROM.

Port 1 to STM32F427 BIST controller;

Port 2 to Cypress CX3 MIPI CSI-2 camera controller;

Port 3 to user XMC rear I/O;

Port 4 to front panel.

MIPI CSI-2 Digitizer **Cypress CX3** USB 3.0 based controller for MIPI CSI-2 1-4 lanes captures high resolution camera input.

Power Requirements MerlinPXC easily exceeds the nominal power limits of PMC (7.5W). XMC is controlled by the amount of available cooling and host power supply capabilities. In order to achieve full operability, the MerlinPXC/2 requires:

Host Bus	Voltage Input	Idle*	Peak Operation*
PMC/XMC	3.3V	0.5A	2A
PMC	5V	1.75A	6.85A
XMC	VPWR=5V	1.75A	6.85A
	VPWR=12V	1.1A	3A

**** Doesn't include power drawn through I/O connectors.***

Power-management: With the proper software, the graphics controlled can power-down unused functions.

Front Panel I/O Connectors MerlinPXC/1V: Single VGA

MerlinPXC/1D: 4x Mini DisplayPort (mDP)

MerlinPXC/2: 4x mDP, MIPI, Micro AB USB 3.0

Rear I/O Connectors MerlinPXC/1V: PMC Pn4, XMC Pn6

MerlinPXC/1D: PMC Pn4, XMC Pn6

MerlinPXC/2: PMC Pn4, XMC Pn6

2.5 Specifications Unique to MerlinMTX

Merlin Graphics Processor: AMD E8860 Multi-Chip Module (MCM).

See Sections 1.3 and 1.4 for details about the E8860.

Display Memory: 2GB GDDR5 on-chip memory.

BIOS PROM: 128KB Flash EEPROM contains the VGA BIOS. Second EEPROM can be installed for customer use (special order).

Graphics Outputs: ***All channels can be active at any time***

1x DisplayPort on PMC Pn4 (Channel C)

2x DVI, single-link on PMC Pn4 (Channels D and F)

XMC/PCIe Bus Interface **IDT 89HPES24T6G2** 6 port PCIe 1.1/2.0 PCIe switch; each port is x4 PCIe lanes.

Ports 0&1: XMC only: x4 or x8, PCIe 2.0;
power save options: x4 only, PCIe 1.1;

Ports 2&3: connected to E8860, x4 or x8, PCIe 2.0;
power save options: x4 only, PCIe 1.1;

Port 4: not used

Port 5: connected to CX25858, x1, PCIe 1.1

Video/Audio Digitizer **Conexant CX25858**, Up to 8 NTSC/PAL Composite Video In and 8 Audio In, all channels can be active at once. As implemented on MerlinMTX, a maximum of 4 video in and 2 audio is possible. Video capture mode is 4:2:2 or 4:1:1, choice of NTSC or PAL affects all inputs; pairs of audio inputs can be configured for stereo. BIOS PROM.

Power Requirements MerlinMTX easily exceeds the nominal power limits of PMC (7.5W). XMC is controlled by the amount of available cooling and host power supply capabilities. In order to achieve full operability, the MerlinMTX requires:

Host Bus	Voltage Input	Idle*	Peak Operation*
PMC/XMC	3.3V	0.5A	2A
PMC	5V	1.75A	6.85A
XMC	VPWR=5V	1.75A	6.85A
	VPWR=12V	1.1A	3A

**** Doesn't include power drawn through I/O connectors.***

Power-management: With the proper software, the graphics controlled can power-down unused functions.

Rear I/O Connectors PMC Pn4

Figure 2-1 Graphical Illustration of Display Formats

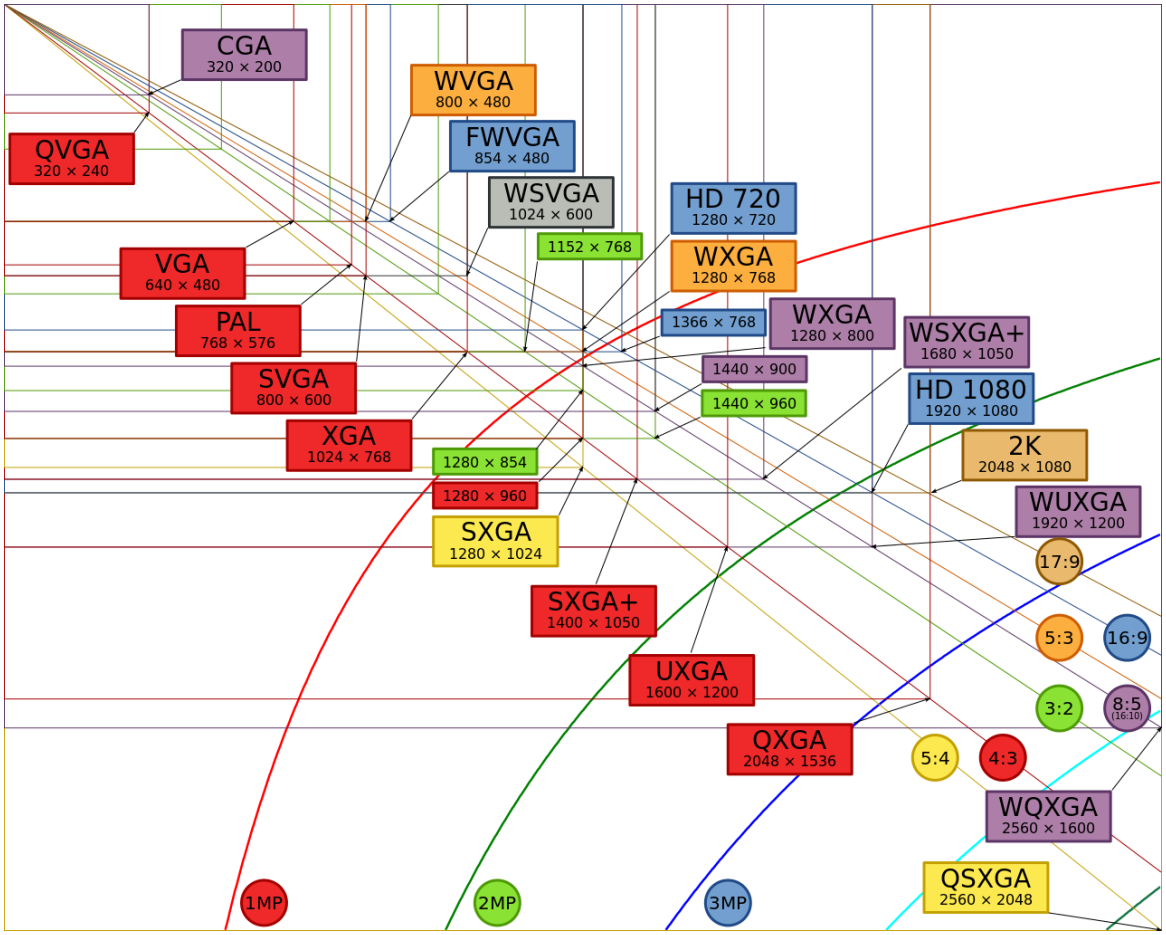


Image courtesy: http://en.wikipedia.org/wiki/File:Vector_Video_Standards2.svg

2.6 Device Codes

2.6.1 PCI Vendor and Device IDs

The PCI Vendor and Device IDs provide a way for the host OS to uniquely identify each device plugged into the PCI or PCIe bus.

In the case of the Agate and Merlin, all of the on-board devices are isolated from the host through one (PCIe) or two (PCI) bridge devices. This means that when you run a PCI map on the devices on your system, the Agate or Merlin devices appear several layers into the map.

Typical maps for PCIe x4 and x4 are shown in the following figures.

Figure 2-2 PCIe x4 Device Map

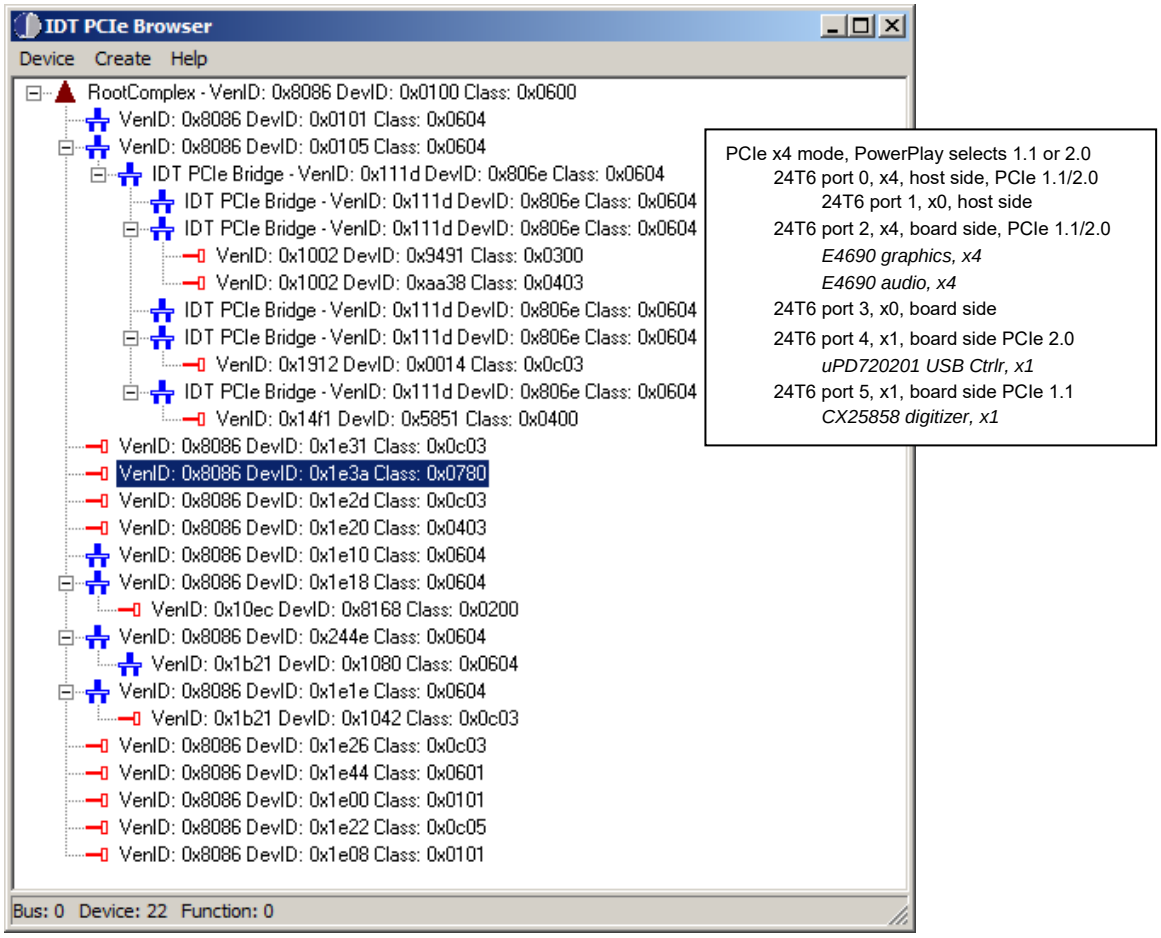


Figure 2-3 PCIe x8 Device Map

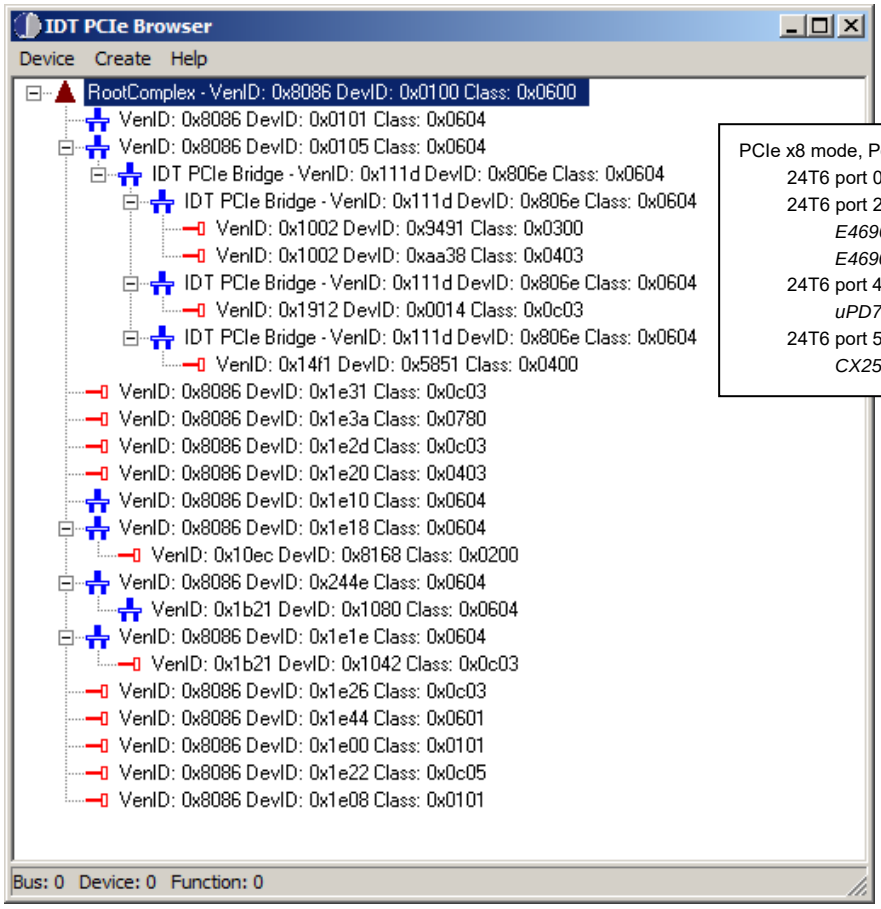


Table 2-3 PCI Vendor and Device IDs

Agate/ Merlin	Vendor	Device	Vendor ID	Device ID	BIOS
Agate	AMD	E4690 graphics E4690 audio ctlr E4690 audio codec	0x1002	0x9491 0xAA38 0xAA01	yes
Merlin	AMD	E8860 graphics E8860 audio ctlr E8860 audio codec	0x1002	0x6822 0xAA90 0xAA01	yes
Agate/MerlinMTX	Conexant	CX25858	0x14F1	0x5851	yes
All	IDT	89HPES24T6G2	0x111D	0x806E	opt
Agate/MerlinPXC	Pericom	PI7C9X130	0x12D8	0xE130	no
Agate/MerlinPXC	Renesas	uPD720201	0x1912	0x0014	yes

2.6.2 JTAG Device Strings

The STM ISM program can scan the JTAG string and report the device codes. This is a handy way to verify that all the devices in the string are actually working. Of course, this doesn't cover all the devices on the board but it does get many of the important ones.

If you plug an external JTAG programming device in, say for the Lattice PLDs, you have to create a chain file of all the devices in the JTAG string or you won't be able to talk to any of them. You have to bypass the non-Lattice parts and in addition to entering the JTAG BYPASS command, you have to load the register width and bypass code.

If you use the Lattice ispVM program and program cable, use the parallel cable and the USB-based one doesn't work correctly with any of the Agate or Merlin boards for reasons unknown.

Except for Cypress, which doesn't release bsdl flies for the CX3 or FX3, you can extract the JTAG ID Code Register value from the manufacturer's .bsdl file. It is of the form:

JTAG IDCODE: Little Endian (bit 0 = LSB)

0x[1 digit]	&	Version Number
0x[4 digit]	&	Part Number
0x[3 bits, 2 digits]	&	Manufacturer ID
"1"		Bit 0, Required by IEEE Std. 1149.1-1990

Thus: [vvvv pppp pppp pppp pppp bbb mmmm mmmm 1] or

In hex, it would be: 0x V P3 P2 P1 P0 [bbbm] M1 [mmm1]

Table 2-4 JTAG Scan Code Information

Agate/ Merlin Present	JTAG String Order	Manufacturer	Device	JTAG ID Code Register Value	JTAG Bypass
Agate/MerlinPXC	1	Lattice	LC4128ZE100	0x01812043	
Agate/MerlinPXC	2	Pericom	PI7C9X130	0x1013047F	5 [11111]
All	3	IDT	89HPES24T6G2	0x2806E067	6 [111111]
Agate/MerlinPXC	4	Cypress	CYUSB3065 (CX3)	0x07926069	4 [1111]
Agate/MerlinPXC	5	Lattice	LC4256ZE100	0x01816043	
Agate	6	Cypress	CYUSB3013 (FX3)	0x07926069	4 [1111]
All	7	Lattice	LC4064ZE48	0x0180E043	
	8*	AMD	E4690 or E8860	0x0948031F	

* this device may not appear in the STM JTAG Scan

2.6.3 I^2C and SPI Devices

I^2C is a two-wire system originated many years ago by Philips. I^2C and its derivative, SMBus, like USB, Ethernet, and RS-232, remain reliable standard communication protocols of long durability. While there are some differences between I^2C and SMB, for the purposes of the Agate and Merlin designs, the two can be and are used on a common bus

There are many devices on the Agate or Merlin that have I^2C or SMBus device addresses.

There are several ways to access most of the I^2C devices on the Agate or Merlin:

a) via the STM on-board diagnostic processor (all boards);

b) via the CX3 (AgatePXC, MerlinPXC);

c) via the FX3 (AgatePXC);

d) via the host CPU, using "fake I^2C", which uses open-collector programmed GPIO bits in the 24T6 to simulate simple I^2C. Rastergraf has a DOS program that implements this method;

In some cases, a particular I^2C is also accessed by the host CPU:

XMC VITA 42 EEPROM

a) via the XMC host processor during boot-up

b) via the STM, CX3, FX3, or "fake I^2C";

CX25858 BOOT EEPROM

a) via the CX25858 private I^2C bus during boot-up

b) via the STM, CX3, FX3, or "fake I^2C";

In the case of the XMC VITA 42 EEPROM, a PCA9541A arbitrates access between the XMC host and the on-board devices. On power-up, the PCA9541A always gives priority access to the Host CPU since the EEPROM is used to help set starting conditions for the system and needs to know the characteristics of each plug-in board.

For more information, consult the VITA/ANSI 42.0 and 42.3 Specifications:

http://shop.vita.com/ANSI-VITA-420-2008-R2014-XMC-AV420.htm

http://shop.vita.com/ANSI-VITA-423-2006-R2014-XMC-PCI-Express-Protocol-Layer-Std-AV423.htm

Table 2-5 AgatePXC (Rev 2) I²C Slave Device Addresses

Device	Function	PLOC	I²C Address	I²C Bus	Controller
CYUSB3065-BZX	CX3 MIPI Ctlr	U012C5	0x0E	GP	reserved – do not access
CYUSB3013-BZX	FX3 ADV Ctlr	U011H2	0x0E	GP	reserved – do not access
LC4128ZE-A192	PLD	U012M6	0x20-2A	GP	ST, 24T6, CX3, FX3
LC4256ZE-A193	PLD	U012C1	0x30-3A	GP	ST, 24T6, CX3, FX3
LC4064ZE-A194	PLD	U012H4	0x3C, 3E	GP	ST, 24T6, CX3, FX3
ICS1526	PLL	U011H5	0x4C	GP	ST, 24T6, CX3, FX3
ADV7441 Map 0-3	RGBHV/DVI	U012J1	0x42/46/4A/4E	GP/FX3	ST, 24T6, CX3, FX3
ADV7441 Map 4-7	RGBHV/DVI	U012J1	0x42/46/4A/4E	GP/FX3	ST, 24T6, CX3, FX3
MIPI Camera	MIPI I²C Buffer	U022B6	0x78 (+)	GP	ST, 24T6, CX3, FX3
E4690	GPU	U011E1	0x82	GP	ST, 24T6, CX3, FX3
LM75BDP	Temp@PwrSup	U011M2	0x90	GP	ST, 24T6, CX3, FX3
ADS1015	V/I ADC	U022M4	0x92	GP	ST, 24T6, CX3, FX3
LM63CIMA	Temp@GPU	U011C2	0x98	GP	ST, 24T6, CX3, FX3
24LC02B	CX25858 BOOT	U022C3	0xA0	GP/CX	ST, 24T6, CX3, FX3, CX*
24LC256	Agate VPD	U012K6	0xA8	GP	ST, 24T6, CX3, FX3
24LC02B !	XMC IPMI PROM	U022K4	0xA[slot]	GP/XMC	ST, 24T6, CX3, FX3, XMC
PI7C9X130	PCI Bridge	U011J5	0xC0	GP	ST, 24T6, CX3, FX3
CY22393	Master Clock	U011D4	0xD2	GP	ST, 24T6, CX3, FX3
ICS9DB403D	PCIe Clock Bfr	U011H5	0xDC	GP	ST, 24T6, CX3, FX3
IDTHPES24T6G2	PCIe Switch	U012F5	0xEE	GP	ST, 24T6, CX3, FX3
PCA9541A	I²C Mux	U012K5	0xF[slot]	GP/XMC	ST, 24T6, CX3, FX3, XMC
STM32F427VIT6	Local CPU	U011C5	programmable	GP	24T6, CX3, FX3

* CX25858-side programming requires Windows app and modified CX2585 driver

\+ Slave Address can be changed in register 0x3100. 0x78 is specified in the MIPI standard but it appears that not every manufacturer abides by that address.

! This may not be programmed correctly. Contact Rastergraf if you have problems.

Table 2-6 AgatePXC (Rev 2) I^2C Masters

Device	Function	PLOC
STM32F427VIT6	Local CPU	U011C5
CYUSB3065-BZX	CX3 MIPI CSI-2 Controller	U012C5
CYUSB3013-BZX	FX3 ADV7441A Controller	U011H2
IDTHPES24T6G2	PCIe Switch (GPIO [1:0])	U012F5

Table 2-7 AgatePXC (Rev 2) SPI Devices

Device	Function	PLOC	Controller
M25P10-AVMN6TP	E4690 BIOS PROM	U021B1	Windows app
M25P10-AVMN6TP	uPD720201 BIOS PROM	U012D4	Windows app
M25P40-VMN6TPB	CX3 BIOS PROM	U022D5	Windows app
M25P40-VMN6TPB	FX3 BIOS PROM	U011J3	Windows app

Table 2-8 MerlinPXC I²C Slave Device Addresses

Device	Function	PLOC	I²C Address	I²C Bus	Controller
CYUSB3065-BZX	CX3 MIPI Ctlr	U012C5	0x0E	GP	reserved – do not access
LC4128ZE-A192	PLD	U012M6	0x20-2A	GP	ST, 24T6, CX33
LC4064ZE-A194	PLD	U012H4	0x3C, 3E	GP	ST, 24T6, CX3
MIPI Camera	MIPI I²C Buffer	U012A6	0x78 (+)	GP	ST, 24T6, CX3
E8860	GPU	U011E1	0x82	GP	ST, 24T6, CX3
LM75BDP	Temp@PwrSup	U011M2	0x90	GP	ST, 24T6, CX3
ADS1015	V/I ADC	U022M4	0x92	GP	ST, 24T6, CX3
LM63CIMA	Temp@GPU	U011E5	0x98	GP	ST, 24T6, CX3
24LC256	Merlin VPD	U012K6	0xA8	GP	ST, 24T6, CX3
24LC02B !	XMC IPMI PROM	U022K4	0xA[slot]	GP/XMC	ST, 24T6, CX3, XMC
PI7C9X130	PCI Bridge	U011J5	0xC0	GP	ST, 24T6, CX3
CY22393	Master Clock	U011C4	0xD2	GP	ST, 24T6, CX3
ICS9DB403D	PCIe Clock Bfr	U011H5	0xDC	GP	ST, 24T6, CX3
IDTHPES24T6G2	PCIe Switch	U012F5	0xEE	GP	ST, 24T6, CX3,
PCA9541A	I²C Mux	U012K5	0xF[slot]	GP/XMC	ST, 24T6, CX3, XMC
STM32F427VIT6	Local CPU	U011C5	programmable	GP	24T6, CX3

+ Slave Address can be changed in register 0x3100. 0x78 is specified in the MIPI standard but it appears that not every manufacturer abides by that address.

! This may not be programmed correctly. Contact Rastergraf if you have problems.

Table 2-9 MerlinPXC I²C Masters

Device	Function	PLOC
STM32F427VIT6	Local CPU	U011C5
CYUSB3065-BZX	CX3 MIPI CSI-2 Controller	U012C5
IDTHPES24T6G2	PCIe Switch (GPIO [1:0])	U012F5

Table 2-10 MerlinPXC SPI Devices

Device	Function	PLOC	Controller
M25P10-AVMN6TP	E8860 BIOS PROM	U022C3	Windows app
M25P10-AVMN6TP	uPD720201 BIOS PROM	U012E5	Windows app
M25P40-VMN6TPB	CX3 BIOS PROM	U012D5	Windows app

Table 2-11 MerlinMTX I²C Slave Device Addresses

Device	Function	PLOC	I²C Address	I²C Bus	Controller
LC4064ZE-A194	PLD	U012H4	0x3C, 3E	GP	ST, 24T6
E8860	GPU	U011E1	0x82	GP	ST, 24T6
LM75BDP	Temp@PwrSup	U011M2	0x90	GP	ST, 24T6
ADS1015	V/I ADC	U022M4	0x92	GP	ST, 24T6
LM63CIMA	Temp@GPU	U011E5	0x98	GP	ST, 24T6
24LC02B	CX25858 BOOT	U021H2	0xA0	GP/CX	ST, 24T6, CX*
24LC256	Merlin VPD	U012K6	0xA8	GP	ST, 24T6
24LC02B !	XMC IPMI PROM	U022K4	0xA[slot]	GP/XMC	ST, 24T6, XMC
CY22393	Master Clock	U011C4	0xD2	GP	ST, 24T6
ICS9DB403D	PCIe Clock Bfr	U011H5	0xDC	GP	ST, 24T6
IDTHPES24T6G2	PCIe Switch	U012F5	0xEE	GP	ST, 24T6
PCA9541A	I²C Mux	U012K5	0xF[slot]	GP/XMC	ST, 24T6, XMC
STM32F427VIT6	Local CPU	U011C5	programmable	GP	24T6

* CX25858-side programming requires Windows app and modified CX2585 driver

! This may not be programmed correctly. Contact Rastergraf if you have problems.

Table 2-12 MerlinMTX I²C Masters

Device	Function	PLOC
STM32F427VIT6	Local CPU	U011C5
IDTHPES24T6G2	PCIe Switch (GPIO [1:0])	U012F5

Table 2-13 MerlinMTX SPI Devices

Device	Function	PLOC	Controller
M25P10-AVMN6TP	E8860 BIOS PROM	U022C3	Windows app

2.6.4 USB Vendor and Device IDs (AgatePXC/MerlinPXC)

This section only applies to the Cypress FX3 and/or CX3 SuperSpeed peripherals used on the Agate and MerlinPXC.

The firmware that runs in the FX3 or CX3 has a unique USB identifier that allows system software to know what the device is and, ideally, the nature of the firmware that it is running. It does this by means of a Vendor ID and a Product ID. Cypress has a unique Vendor ID assigned to it by usb.org and Cypress has assigned a Product IDs for its USB devices.

As listed in the current Windows 10 cyusb3.inf file they have:

VID_XXXX&PID_XXXX.DeviceDesc="Cypress USB3.0 Generic Driver"
VID_04B4&PID_00F0.DeviceDesc="Cypress FX3 USB BulkloopExample Device"
VID_04B4&PID_00F1.DeviceDesc="Cypress FX3 USB StreamerExample Device"
VID_04B4&PID_00F3.DeviceDesc="Cypress FX3 USB BootLoader Device"
VID_04B4&PID_4720.DeviceDesc="Cypress FX3 USB BootProgrammer Device"
VID_04B4&PID_00B0.DeviceDesc="Cypress Bay USB Boot Device"
VID_04B4&PID_00BC.DeviceDesc="Cypress Benicia USB Boot Device"
VID_04B4&PID_FFF1.DeviceDesc="Cypress FX3 Workshop Lab1_UsbEnumeration"
VID_04B4&PID_FFF2.DeviceDesc="Cypress FX3 Example device 1"
VID_04B4&PID_FFF3.DeviceDesc="Cypress FX3 Example device 2"
VID_04B4&PID_0053.DeviceDesc="Cypress SD3 USB Boot Device"
VID_04B4&PID_0082.DeviceDesc="Cypress FX2LP Development board"
VID_04B4&PID_0095.DeviceDesc="Cypress FX2LP USB-JTAG debug probe"
VID_04B4&PID_1004.DeviceDesc="Cypress FX2LP Sample Device"
VID_04B4&PID_8613.DeviceDesc="Cypress FX2LP No EEPROM Device"
VID_04B4&PID_1003.DeviceDesc="Cypress FX2LP StreamerExample Device"
VID_04B4&PID_6823.DeviceDesc="Cypress EZ-USB NX2LP-Flex BootLoader Device"
VID_04B4&PID_4617.DeviceDesc="Cypress EZ-USB NX2LP-Flex Unprogrammed NAND"
VID_04B4&PID_4611.DeviceDesc="Cypress FX2 USB Storage Adapter"
VID_04B4&PID_6830.DeviceDesc="Cypress AT2 USB Storage Adapter"
VID_04B4&PID_00A1.DeviceDesc="Cypress Antioch USB Boot Device"
VID_04B4&PID_00A2.DeviceDesc="Cypress Astoria No EEPROM Device"
VID_04B4&PID_6473.DeviceDesc="Cypress EZ-USB FX1 No EEPROM Device"
VID_04B4&PID_00FA.DeviceDesc="USB-Serial MFG mode"
VID_04B4&PID_0072.DeviceDesc="Cypress CCGx PD Analyzer"
VID_04B4&PID_0002&MI_02.DeviceDesc="USB-Serial (Single Channel) Vendor MFG"
VID_04B4&PID_0004&MI_00.DeviceDesc="USB-Serial (Single Channel) Vendor 1"
VID_04B4&PID_0004&MI_01.DeviceDesc="USB-Serial (Single Channel) Vendor MFG"
VID_04B4&PID_0003&MI_02.DeviceDesc="USB-UART LP Vendor MFG"
VID_04B4&PID_0006&MI_00.DeviceDesc="USB-UART LP Vendor 1"
VID_04B4&PID_0006&MI_01.DeviceDesc="USB-UART LP Vendor MFG"
VID_04B4&PID_0005&MI_04.DeviceDesc="USB-Serial (Dual Channel) Vendor MFG"
VID_04B4&PID_0007&MI_02.DeviceDesc="USB-Serial (Dual Channel) Vendor 1"
VID_04B4&PID_0007&MI_03.DeviceDesc="USB-Serial (Dual Channel) Vendor MFG"
VID_04B4&PID_0009&MI_00.DeviceDesc="USB-Serial (Dual Channel) Vendor 1"
VID_04B4&PID_0009&MI_03.DeviceDesc="USB-Serial (Dual Channel) Vendor MFG"
VID_04B4&PID_000A&MI_00.DeviceDesc="USB-Serial (Dual Channel) Vendor 1"
VID_04B4&PID_000A&MI_01.DeviceDesc="USB-Serial (Dual Channel) Vendor 2"
VID_04B4&PID_000A&MI_02.DeviceDesc="USB-Serial (Dual Channel) Vendor MFG"
VID_04B4&PID_000B&MI_01.DeviceDesc="Cypress USB-I2C PTP Bridge MFG"
VID_04B4&PID_521A&MI_00.DeviceDesc="Billboard USB-I2C Bridge Vendor 1"
VID_04B4&PID_521A&MI_01.DeviceDesc="Billboard USB-I2C Bridge Vendor MFG"
VID_04B4&PID_5218&MI_00.DeviceDesc="Billboard USB-I2C Bridge Vendor 1"
VID_04B4&PID_5218&MI_01.DeviceDesc="Billboard USB-I2C Bridge Vendor 2"
VID_04B4&PID_5218&MI_02.DeviceDesc="Billboard Bridge Vendor MFG"
VID_04B4&PID_5219&MI_00.DeviceDesc="Billboard USB-I2C Bridge Vendor 1"
VID_04B4&PID_5219&MI_03.DeviceDesc="Billboard Bridge Vendor MFG"
VID_04B4&PID_00FB&MI_02.DeviceDesc="USB-Serial (Single Channel) Vendor MFG"
VID_04B4&PID_0033&MI_01.DeviceDesc="USB-Serial (Single Channel) Vendor MFG"
VID_04B4&PID_6560.DeviceDesc="Cypress Hub USB Manufacturing Driver"
VID_04B4&PID_6572.DeviceDesc="Cypress HX2VL(Multi-TT) DVK"
VID_04B4&PID_6570.DeviceDesc="Cypress HX2VL(Multi-TT) DVK"

If you are going to use the Cypress SDK software, you must retain the Cypress Vendor ID (0x0484). See this article.

You can change the Product ID (PID) when you build your own software application to run in the CX3 or FX3.

That said, as discussed in Section 8.8.2.3 and Section 8.8.3, there are hazards to changing these assignments for Windows 10.

Suffice it to say that unless you are an experienced Windows system programmer and are in possession of an EV SSL certificate, you do NOT want to touch the cysub3.inf at all.

If you want to use a different USB PID, you could most likely safely use PID_FFF2 or PID_FFF3. Or, take a chance and use some other PID that will never be used in your system. "Your mileage may vary".

Rastergraf uses the following codes in its preloaded "Blinker" program.

Note that for both the FX3 and CX3, the Blinker program also serves as a standard Cypress FX3 USB BootLoader Device. The only difference it that the chip runs a little routine that turns its associated LED off and on.

Table 2-14 Cypress FX3 and CX3 USB ID Codes

Device	Vendor ID	Product ID	Cypress Description
FX3	0x04B4	0x00F3	Cypress FX3 USB BootLoader Device *
CX3	0x04B4	0xFFF3	Cypress FX3 Example device 2 *

* the code that is running is Cypress FX3 USB BootLoader Device and will show as a bootloader in the Cypress Control Center.

2.7 AgatePXC (Rev 2) STM32F427 Port Assignment

The ST Micro STM32F427 is a 100-pin TQFP 32-bit ARM processor with 2MB on-chip Flash EPROM. It is used to monitor on-board devices and to support the built-in debugger program. It allows you to dig into the board in ways that aren't possible from the host.

The following table documents the port bit assignments.

Table 2-15 Agate STM32F427 Port Bit Assignment

Port Name	Port Pin	Agate Signal Name	STM Name	Description Agate Rev 2 6/8/2015
PA_00	23	PA0		Wakeup/re-start switch
PA_01	24	ADV_HS_R	TIM2_CH2 / ADC123_IN1	ADV Hsync
PA_02	25	STM_VDD_12F	ADC123_IN2	ADC input to measure FX3 VDD_12 (1.2V)
PA_03	26	STM_VDDIO_CX	ADC123_IN3	ADC input to measure CX3 VDDIO (switched 3.3V)
PA_04	29	JTAG_TMS	SPI3_NSS / ADC12_IN4	use SPI3 for JTAG
PA_05	30	ADV_VS_R	TIM2_CH1 / ADC12_IN5	ADV Vsync
PA_06	31	HSYNC_DAC1	TIM3_CH1 / ADC12_IN6	DAC 1 Hsync
PA_07	32	HSYNC_DAC2	TIM3_CH2 / ADC12_IN7	DAC 2 Hsync
PA_08	67	CX3_SCL	I2C3_SCL	to CX3 bit-bang I^2C, GPIO[25] (not implemented)
PA_09	68	STM_USB_VBUS	OTG_VBUS	direct read of USB Power (dup of PB_13)
PA_10	69	FP_PON		Backup Enable U012B4 power switch
PA_11	70	STM_FS_DN	OTG_FS_DM	USB for DFU and edge connector for debugger (std ISM)
PA_12	71	STM_FS_DP	OTG_FS_DP	USB for DFU and edge connector for debugger (std ISM)
PA_13	72	STM_DIO	JTMS-SWDIO	SWD ST Micro Debugger Port
PA_14	76	STM_CLK	JTCK-SWCLK	SWD ST Micro Debugger Port
PA_15	77	(reserved)	JTDI	
PB_00	35	STM_VDD_18	ADC12_IN8	ADC input to measure VDD_18 (1.8V)
PB_01	36	STM_VDD_C	ADC12_IN9	ADC input to measure VDD_C (0.9V - 1.05V)
PB_02	37	BOOT1	BOOT1	not connected except 1K pulldown to GND
PB_03	89	(reserved)	(JTDO)	
PB_04	90	(reserved)	(NJTRST)	
PB_05	91	STM_HS_PFTL		Fault flag from HS USB power switch
PB_06	92	JTAG_TRST_L		part of STM driving JTAG signal set
PB_07	93	STM_HS_VBON		Enable HS USB power switch

PB_08	95	GP_SCL	I2C1_SCL	primary I^2C (GP) CLK
PB_09	96	GP_SDA	I2C1_SDA	primary I^2C (GP) DATA
PB_10	47	(not used)	I2C2_SCL	
PB_11	48	(not used)	I2C2_SDA	
PB_12	51	STM_HS_ID	OTG_HS_ID	host USB port ID bit
PB_13	52	STM_USB_VBUS	OTG_VBUS	direct read of USB Power (dup of PA_09)
PB_14	53	STM_HS_DN	OTG_HS_DM	allow host to talk to STM via uPD720201 port 1 (alt ISM)
PB_15	54	STM_HS_DP	OTG_HS_DP	allow host to talk to STM via uPD720201 port 1 (alt ISM)
PC_00	15	STM_VDD_10	ADC123_IN10	ADC input to measure VDD_10 (1.05V)
PC_01	16	STM_VDD_25	ADC123_IN11	ADC input to measure VDD_25 (2.5V)
PC_02	17	STM_VDD_12C	ADC123_IN12	ADC input to measure CX3 VDD_12 (1.2V)
PC_03	18	STM_VDD_11	ADC123_IN13	ADC input to measure VDD_11 (1.1V)
PC_04	33	STM_VDDR3	ADC12_IN14	ADC input to measure VDDR3 (switched 3.3V)
PC_05	34	STM_VFP	ADC12_IN15	ADC input to measure the MIPI power (usually 3.3V)
PC_06	63	(not used)		
PC_07	64	(not used)		
PC_08	65	CX3_LED_N		Can drive CX3 LED. Normally, float this pin
PC_09	66	CX3_SDA	I2C3_SDA	CX3 bit-bang I^2C, GPIO[20] (not implemented)
PC_10	78	STM_TCK	SPI3_SCK	Drive JTAG loop using SPI3 for JTAG
PC_11	79	GPIO28_TDO_R	SPI3_MISO (master input)	this is end of the JTAG loop
PC_12	80	U012M6_TDI	SPI3_MOSI (master output)	this is the beginning of the JTAG loop
PC_13	7	(not used)		
PC_14	8	(not used)		
PC_15	9	(not used)		
PD_00	81	(not used)		
PD_01	82	STM_MBISTH		enables JTAG mux so that STM can run JTAG, pulldown
PD_02	83	STM_ADINTN		low active interrupt from ADS1015 ADC, pullup
PD_03	84	I2C_FLAG_N		handshaking flag to 24T6 for I^2C handoff to host
PD_04	85	YELLED_N		(active low), pullup
PD_05	86	GRNALED_N		(active low), pullup
PD_06	87	REDLED_N		(active low), pullup
PD_07	88	CX_INTN		interrupt from the CX3, uses CX3 INT# pin (no pullup on PCB, use STM pullup)
PD_08	55	(not used)		
PD_09	56	(not used)		
PD_10	57	(not used)		
PD_11	58	FX3_REQN		request to FX3 from STM, FX3 GPIO[45] , pullup
PD_12	59	GRNBLED_N	TIM4_CH1	heartbeat LED, (active low), pullup
PD_13	60	(not used)		

PD_14	61	(not used)		
PD_15	62	FX_INTN		interrupt from the FX3, uses FX3 INT# pin, pullup
PE_00	97	CX3_UART_TX	UART8_RX	Enable ISM to talk to the CX3 UART (not implemented)
PE_01	98	CX3_UART_RX	UART8_TX	Enable ISM to talk to the CX3 UART (not implemented)
PE_02	1	X3_RSTN		active low force reset of CX3/FX3/ADV, pullup
PE_03	2	SPARE		not used, connects to all PLDs, pullup
PE_04	3	CX3_REQN		request to CX3 from STM, CX3 GPIO[18] , pullup
PE_05	4	OTMP_LED_N		OTMP LED, input but we could drive for attention, pullup
PE_06	5	(not used)		
PE_07	38	FX3_UART_TX	UART7_RX	Enable ISM to talk to the FX3 UART (not implemented)
PE_08	39	FX3_UART_RX	UART7_TX	Enable ISM to talk to the FX3 UART (not implemented)
PE_09	40	VSYNC_DAC1	TIM1_CH1	DAC 1 Vsync
PE_10	41	STM_I2C_BUFEN		Enable I^2C buffers so that GP I^2C can see CX25858 PROM, pulldown
PE_11	42	VSYNC_DAC2	TIM1_CH2	DAC 2 Vsync
PE_12	43	(not used)		
PE_13	44	(not used)		
PE_14	45	(not used)		
PE_15	46	(not used)		
PH_00	12	CPU_CLKR		STM Master Clock Input - 19.2 MHz
PH_01	13	(reserved)		

2.8 MerlinPXC STM32F427 Port Assignment

The ST Micro STM32F427 is a 100-pin TQFP 32-bit ARM processor with 2MB on-chip Flash EPROM. It is used to monitor on-board devices and to support the built-in debugger program. It allows you to dig into the board in ways that aren't possible from the host.

The following table documents the port assignments.

Table 2-16 MerlinPXC STM32F427 Port Assignment

Port Name	Port Pin	Merlin Signal Name	STM Name	Description Merlin Rev 0 6/17/2015
PA_00	23	PA0		Wakeup/re-start switch
PA_01	24	STM_VDDCI	TIM2_CH2 / ADC123_IN1	Merlin Secondary Core Voltage (0.90/0.95)
PA_02	25	STM_VDD_095	ADC123_IN2	ADC input to measure Merlin DP supply (0.95V)
PA_03	26	STM_VDDIO_CX	ADC123_IN3	ADC input to measure CX3 VDDIO (switched 3.3V)
PA_04	29	JTAG_TMS	SPI3_NSS / ADC12_IN4	Use SPI3 for JTAG
PA_05	30	(not used)	TIM2_CH1 / ADC12_IN5	
PA_06	31	HSYNC_DAC1	TIM3_CH1 / ADC12_IN6	DAC 1 Hsync
PA_07	32	(not used)	TIM3_CH2 / ADC12_IN7	
PA_08	67	CX3_SCL	I2C3_SCL	to CX3 bit-bang I^2C, GPIO[25] (not implemented)
PA_09	68	STM_USB_VBUS	OTG_VBUS	direct read of USB Power (dup of PB_13)
PA_10	69	FP_PON		Backup Enable U012B4 power switch
PA_11	70	STM_FS_DN	OTG_FS_DM	USB for DFU and edge connector for debugger (std ISM)
PA_12	71	STM_FS_DP	OTG_FS_DP	USB for DFU and edge connector for debugger (std ISM)
PA_13	72	STM_DIO	JTMS-SWDIO	SWD ST Micro Debugger Port
PA_14	76	STM_CLK	JTCK-SWCLK	SWD ST Micro Debugger Port
PA_15	77	(not used)	JTDI	
PB_00	35	STM_VDD_18	ADC12_IN8	ADC input to measure VDD_18 (1.8V)
PB_01	36	STM_VDD_C	ADC12_IN9	ADC input to measure VDD_C (0.805V - 0.980V)
PB_02	37	BOOT1	BOOT1	not connected except 1K pulldown to GND
PB_03	89	(reserved)	(JTDO)	
PB_04	90	(reserved)	(NJTRST)	
PB_05	91	STM_HS_PFTL		Fault flag from HS USB power switch
PB_06	92	JTAG_TRST_L		part of STM driving JTAG signal set
PB_07	93	STM_HS_VBON		Enable HS USB power switch

PB_08	95	GP_SCL	I2C1_SCL	GP I^2C CLK
PB_09	96	GP_SDA	I2C1_SDA	GP I^2C DATA
PB_10	47	(not used)	I2C2_SCL	
PB_11	48	(not used)	I2C2_SDA	
PB_12	51	STM_HS_ID	OTG_HS_ID	host USB port ID bit
PB_13	52	STM_USB_VBUS	OTG_VBUS	direct read of USB Power (dup of PA_09)
PB_14	53	STM_HS_DN	OTG_HS_DM	allow host to talk to STM via uPD720201 port 1 (alt ISM)
PB_15	54	STM_HS_DP	OTG_HS_DP	allow host to talk to STM via uPD720201 port 1 (alt ISM)
PC_00	15	STM_VDD_10	ADC123_IN10	ADC input to measure VDD_10 (1.05V)
PC_01	16	STM_VDD_25	ADC123_IN11	ADC input to measure VDD_25 (2.5V)
PC_02	17	STM_VDD_12C	ADC123_IN12	ADC input to measure CX3 VDD_12 (1.2V)
PC_03	18	STM_VDDR1	ADC123_IN13	ADC input to measure VDDR1 (1.35/1.50)
PC_04	33	STM_VDDR3	ADC12_IN14	ADC input to measure VDDR3 (switched 3.3V)
PC_05	34	STM_VFP	ADC12_IN15	ADC input to measure the MIPI power (usually 3.3V)
PC_06	63	(not used)		
PC_07	64	(not used)		
PC_08	65	CX3_LED_N		Can drive CX3 LED. Normally, float this pin
PC_09	66	CX3_SDA	I2C3_SDA	CX3 bit-bang I^2C, GPIO[20] (not implemented)
PC_10	78	STM_TCK	SPI3_SCK	Drive JTAG loop using SPI3 for JTAG
PC_11	79	GPIO28_TDO_R	SPI3_MISO (master input)	this is end of the JTAG loop
PC_12	80	U012M6_TDI	SPI3_MOSI (master output)	this is the beginning of the JTAG loop
PC_13	7	(not used)		
PC_14	8	(not used)		
PC_15	9	(not used)		
PD_00	81	(not used)		
PD_01	82	STM_MBISTH		enables JTAG mux so that STM can run JTAG, pulldown
PD_02	83	STM_ADINTN		low active interrupt from ADS1015 ADC, pullup
PD_03	84	I2C_FLAG_N		handshaking flag to 24T6 for I^2C handoff to host
PD_04	85	YELLED_N		(active low), pullup
PD_05	86	GRNALED_N		(active low), pullup
PD_06	87	REDLED_N		(active low), pullup
PD_07	88	CX_INTN		interrupt from the CX3, uses CX3 INT# pin, pullup
PD_08	55	(not used)		
PD_09	56	MIPI_PFTL		power fault on MIPI power switch, pullup
PD_10	57	(not used)		
PD_11	58	(not used)		
PD_12	59	GRNBLED_N	TIM4_CH1	heartbeat LED, (active low), pullup
PD_13	60	(not used)		
PD_14	61	(not used)		

PD_15	62	(not used)		
PE_00	97	CX3_UART_TX	UART8_RX	Enable ISM to talk to the CX3 UART (not implemented)
PE_01	98	CX3_UART_RX	UART8_TX	Enable ISM to talk to the CX3 UART (not implemented)
PE_02	1	X3_RSTN		active low force reset of CX3, pullup
PE_03	2	SPARE		not used, connects to all PLDs, pullup
PE_04	3	CX3_REQN		request to CX3 from STM, CX3 GPIO[18] , pullup
PE_05	4	OTMP_LED_N		OTMP LED, input but we could drive for attention, pullup
PE_06	5	(not used)		
PE_07	38	(not used)		
PE_08	39	(not used)		
PE_09	40	VSYNC_DAC1	TIM1_CH1	DAC 1 Vsync
PE_10	41	STM_I2C_BUFEN		Enable I^2C buffer so that GP I^2C can see CX25858 PROM, pulldown
PE_11	42	(not used)		
PE_12	43	(not used)		
PE_13	44	(not used)		
PE_14	45	CLK_SEL		monitor this pin to know if alt clock set used in CY22393, pullup
PE_15	46	STM_TESTEN		allow STM to put E8860 into test mode. Linked to TESTEN pin by R052C4, R is NOT installed, pulldown
PH_00	12	CPU_CLKR		STM Master Clock Input - 19.2 MHz
PH_01	13	(reserved)		

2.9 MerlinMTX STM32F427 Port Assignment

The ST Micro STM32F427 is a 100-pin TQFP 32-bit ARM processor with 2MB on-chip Flash EPROM. It is used to monitor on-board devices and to support the built-in debugger program. It allows you to dig into the board in ways that aren't possible from the host.

The following table documents the port assignments.

Table 2-17 MerlinMTX STM32F427 Port Assignment

Port Name	Port Pin	Merlin Signal Name	STM Name	Description Merlin Rev 0 6/17/2015
PA_00	23	PA0		Wakeup/re-start switch
PA_01	24	STM_VDDCI	TIM2_CH2 / ADC123_IN1	Merlin Secondary Core Voltage (0.90/0.95)
PA_02	25	STM_VDD_095	ADC123_IN2	ADC input to measure Merlin DP supply (0.95V)
PA_03	26	(not used)	ADC123_IN3	
PA_04	29	JTAG_TMS	SPI3_NSS / ADC12_IN4	Use SPI3 for JTAG
PA_05	30	(not used)	TIM2_CH1 / ADC12_IN5	
PA_06	31	HSYNC_DAC1	TIM3_CH1 / ADC12_IN6	DAC 1 Hsync
PA_07	32	(not used)	TIM3_CH2 / ADC12_IN7	
PA_08	67	(not used)	I2C3_SCL	
PA_09	68	STM_USB_VBUS	OTG_VBUS	direct read of USB Power (dup of PB_13)
PA_10	69	(not used)		
PA_11	70	STM_CON_DN	OTG_FS_DM	USB for DFU and edge connector for debugger (std ISM)
PA_12	71	STM_CON_DP	OTG_FS_DP	USB for DFU and edge connector for debugger (std ISM)
PA_13	72	STM_DIO	JTMS-SWDIO	SWD ST Micro Debugger Port
PA_14	76	STM_CLK	JTCK-SWCLK	SWD ST Micro Debugger Port
PA_15	77	(not used)	JTDI	
PB_00	35	STM_VDD_18	ADC12_IN8	ADC input to measure VDD_18 (1.8V)
PB_01	36	STM_VDD_C	ADC12_IN9	ADC input to measure VDD_C (0.805V - 0.980V)
PB_02	37	BOOT1	BOOT1	not connected except 1K pulldown to GND
PB_03	89	(reserved)	(JTDO)	
PB_04	90	(reserved)	(NJTRST)	
PB_05	91	STM_HS_PFTL		Fault flag from HS USB power switch
PB_06	92	JTAG_TRST_L		part of STM driving JTAG signal set
PB_07	93	STM_HS_VBON		Enable HS USB power switch

PB_08	95	GP_SCL	I2C1_SCL	GP I^2C CLK
PB_09	96	GP_SDA	I2C1_SDA	GP I^2C DATA
PB_10	47	TS_JTAG_MUX	I2C2_SCL	Control E8860 JTAG mux – not implemented
PB_11	48	(not used)	I2C2_SDA	
PB_12	51	STM_HS_ID	OTG_HS_ID	auxiliary USB port
PB_13	52	STM_USB_VBUS	OTG_VBUS	direct read of USB Power (dup of PA_09)
PB_14	53	(not used)	OTG_HS_DM	
PB_15	54	(not used)	OTG_HS_DP	
PC_00	15	STM_VDD_10	ADC123_IN10	ADC input to measure VDD_10 (1.05V)
PC_01	16	STM_VDD_25	ADC123_IN11	ADC input to measure VDD_25 (2.5V)
PC_02	17	(not used)	ADC123_IN12	
PC_03	18	STM_VDDR1	ADC123_IN13	ADC input to measure VDDR1 (1.35/1.50)
PC_04	33	STM_VDDR3	ADC12_IN14	ADC input to measure VDDR3 (switched 3.3V)
PC_05	34	(not used)	ADC12_IN15	
PC_06	63	(not used)		
PC_07	64	(not used)		
PC_08	65	(not used)		
PC_09	66	(not used)	I2C3_SDA	
PC_10	78	STM_TCK	SPI3_SCK	Drive JTAG loop using SPI3 for JTAG
PC_11	79	GPIO28_TDO_R	SPI3_MISO (master input)	this is end of the JTAG loop
PC_12	80	U012M6_TDI	SPI3_MOSI (master output)	this is the beginning of the JTAG loop
PC_13	7	(not used)		
PC_14	8	(not used)		
PC_15	9	(not used)		
PD_00	81	(not used)		
PD_01	82	STM_MBISTH		enables JTAG mux so that STM can run JTAG, pulldown
PD_02	83	STM_ADINTN		low active interrupt from ADS1015 ADC, pullup
PD_03	84	I2C_FLAG_N		handshaking flag to 24T6 for I^2C handoff to host
PD_04	85	YELLED_N		(active low), pullup
PD_05	86	GRNALED_N		(active low), pullup
PD_06	87	REDLED_N		(active low), pullup
PD_07	88	(not used)		
PD_08	55	(not used)		
PD_09	56	(not used)		
PD_10	57	(not used)		
PD_11	58	(not used)		
PD_12	59	GRNBLED_N	TIM4_CH1	heartbeat LED, (active low), pullup
PD_13	60	(not used)		
PD_14	61	(not used)		

PD_15	62	(not used)		
PE_00	97	(not used)	UART8_RX	
PE_01	98	(not used)	UART8_TX	
PE_02	1	(not used)		
PE_03	2	SPARE		not used, connects to PLD, pullup
PE_04	3	(not used)		
PE_05	4	OTMP_LED_N		OTMP LED, input but we could drive for attention, pullup
PE_06	5	(not used)		
PE_07	38	(not used)		
PE_08	39	(not used)		
PE_09	40	VSYNC_DAC1	TIM1_CH1	DAC 1 Vsync
PE_10	41	STM_I2C_BUFEN		Enable buffer so that GP I^2C can see CX25858 PROM, pulldown
PE_11	42	(not used)		
PE_12	43	(not used)		
PE_13	44	(not used)		
PE_14	45	CLK_SEL		monitor this pin to know if alt clock set used in CY22393, pullup
PE_15	46	STM_TESTEN		allow STM to put E8860 into test mode. Linked to TESTEN pin by R052C4, R is NOT installed, pulldown
PH_00	12	CPU_CLKR		STM Master Clock Input - 19.2 MHz
PH_01	13	(reserved)		

2.10 Voltages and Clocks

Many voltages and clocks can be verified by locating the marked pads or pins on Side 2 of the PCB, the side that is exposed when the board is plugged in. Great care must be exercised when poking around a live board. If you zap something, it will not be covered under warranty.

2.10.1 AgatePXC Voltages and Clocks

Power up current 1.5A – 2.A @ 5V, .0.5A @ 3.3V

Table 2-18 Agate Voltages and Clocks

Voltage	Value
VDD_CORE	0.90V -1.05V
VDD_10	1.05V
VDD_11	1.13V
VDD_12C	1.2V
VDD_12F	1.2V
MVDDQ	1.8V
VDD_18	1.8V
VDD_18M	1.8V
VDD_18P	1.8V
VDD_25	2.5V
VDD_25M	2.5V
VDDR3	3.3V

Clock Name	Frequency	Level
CXCLK	48.00MHz	1.8V
CPCLK	27.00MHz	1.8V
FCLK	19.16MHz	3.3V
SCCLK	19.16MHz	3.3V
ADVCLK	28.5MHz	3.3V
USBCLK	24.00MHz	1.8V
PLDCLK	14.318MHz	3.3V
9REF+	100.00MHz	1.0V
PREF-	100.00MHz	1.0V

2.10.2 MerlinPXC Voltages and Clocks

Power up current 1.5A – 2.A @ 5V, .0.5A @ 3.3V

Table 2-19 Merlin Voltages and Clocks

Voltage	Value
VDD_095	0.95V
VDD_10	1.05V
VDD_CORE	0.805 - 0.98V
VDDCI	0.90 or 0.95
VDD_11	1.13V
VDD_12C	1.2V
VDDR1	1.35 or 1.5 (default)
VDD_18	1.8V
VDD_18M	1.8V
VDD_18P	1.8V
VDD_25	2.5V
VDD_25M	2.5V
VDD	3.3V
VDDR3	3.3V
VCC_XMC	5.0V
7VCC	5.0V

Clock Name	Frequency	Level
PLDCLK	14.318MHz	3.3V
SCCLK	19.16MHz	3.3V
USBCLK	24.00MHz	1.8V
GPCLK	27.00MHz	3.3V
X2CLK	100.00MHz	3.3V
9REF+	100.00MHz	1.0V
PREF-	100.00MHz	1.0V

2.10.3 MerlinMTX Voltages and Clocks

Power up current 1.5A – 2.A @ 5V, .0.5A @ 3.3V

Table 2-20 Merlin Voltages and Clocks

Voltage	Value
VDD_095	0.95V
VDD_10	1.05V
VDD_CORE	0.805 - 0.98V
VDDCI	0.90 or 0.95
VDD_11	1.13V
VDD_12C	1.2V
VDDR1	1.35 or 1.5 (default)
VDD_18	1.8V
VDD_18M	1.8V
VDD_18P	1.8V
VDD_25	2.5V
VDD_25M	2.5V
VDD	3.3V
VDDR3	3.3V
VCC_XMC	5.0V
VCC	5.0V

Clock Name	Frequency	Level
CXCLK	48.00MHz	1.8V
PLDCLK	14.318MHz	3.3V
SCCLK	19.16MHz	3.3V
GPCLK	27.00MHz	3.3V
X2CLK	100.00MHz	3.3V
PREF-	100.00MHz	1.0V

2.11 E4690 Configuration Straps

The E4690 is preloaded on power-up with a number of startup parameters called Configuration Straps. They set a variety of functions for the convenience of the board designer.

The straps are implemented with pullup resistors. Some functions can also be changed by the BIOS, but still require a valid default power-up state.

Table 2-21 E4690 Configuration Straps

Signal Name	I/O Pin	Function	Agate
TX_PWRS_ENB	GPIO0	PCIE Full Tx Out Swing En	1
TX_DEEMPH_EN	GPIO1	PCIE XMIT De-Emphasis En	1
BIF_GEN2_EN_A	GPIO2	PCIE Gen2 Enable	1
GPIO5_AC_BATT TEST	GPIO5	Low For Batt/Pwr Save Mode	SW7-2
BIF_VGA DIS	GPIO9	VGA Disable	SW7-1
ROMIDCFG[2:0]	GPIO[13:11]	Numonyx/Micron M25P10A	[101]
BIOS_ROM_EN	GPIO22	Enable Local (not system) BIOS ROM	1
AUD[1:0]	[H:V]SYNC_DAC1	Audio for DisplayPort only	[10]
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	VIP DEVICE Enable	0
BIF_CLK_PM_EN	GPIO8	AMD Reserved - must be 0 on power-up	0
SMS_EN_HARD	HSYNC_DAC2	AMD Reserved - must be 0 on power-up	0
CCBYPASS	GENERICC	AMD Reserved - must be 0 on power-up	0
BIF_RX_PLL_CALIB_BP	GPIO21	AMD Reserved - must be 0 on power-up	0
GPIO_28_TDO	GPIO28	AMD Reserved - must be 0 on power-up	0

2.12 E8860 Configuration Straps

The E8860 is preloaded on power-up with a number of startup parameters called Configuration Straps. They set a variety of functions for the convenience of the board designer.

Most of the straps are encoded using a 4-bit R/C circuit instead of pullup resistors. Some functions can also be changed by the BIOS, but still require a valid default power-up state.

Table 2-22 E8860 MLPS Configuration Straps

Signal Name	Encoded Bit Posn	Function	All Merlin	R/C up	R/C down
Audio Port [2:1]	PS_3[5:4]	[000] to enable all ports	[00]		0.68uF
Reserved	PS_3[3:1]	Must be 0 at reset	[000]		4750
Reserved	PS_2[5]	Must be 1 at reset	[10]		0.01uF
VGA_DIS	PS_2[4]	0 = enable VGA mode			
BIOS_ROM_EN	PS_2[3]	1 = Enable the external BIOS			
Reserved	PS_2[2]	Must be 0 at reset	[100]	4530	4990
Reserved	PS_2[1]	Must be 0 at reset			
TX_DEEMPH_EN	PS_1[5]	1 = Tx de-emphasis enabled	[11]		
TX_PWRS_ENB	PS_1[4]	1 = Full Tx output swing			
Reserved	PS_1[3]	Must be 0 at reset			
Reserved	PS_1[2]	Must be 0 at reset	[000]		4750
PCIE_GEN3	PS_1[1]	0 = no PCIe Gen3			
Audio Port [0]	PS_0[5]	[000] to enable all ports	[01]		0.082uF
Reserved	PS_0[4]	Must be 1 at reset			
ROM_CONFIG[2:0]	PS_0[3:1]	Numonyx/Micron 25P10A	[101]	3240	5620

Table 2-23 E8860 Standard Configuration Straps

Signal Name	I/O Pin	Function	Agate
AUD[1:0]	[H:V]SYNC_DAC1	Audio for DisplayPort only	[10]

2.13 VGA Display Timing

The following tables provide the typical timing for VGA displays.

Table 2-24 BIOS Display Timing Specifications

Active Display	Format	Bits per Pixel	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 400	VGA	8	60 Hz	31.55 kHz	27 MHz

Table 2-25 VGA/Windows Platform Display Timing Specifications

Active Display	VESA Format	Bits per Pixel	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 480	n/a VGA VGA VGA	8, 16, 32	60 Hz 72 Hz 75 Hz 85 Hz	31.5 kHz 37.9 kHz 37.5 kHz 43.4 kHz	25.175 MHz 31.5 MHz 31.5 MHz 36 MHz
800 x 600	SVGA	8, 16, 32	60 Hz 72 Hz 75 Hz 85 Hz	37.9 kHz 48.1 kHz 46.9 kHz 53.7 kHz	40 MHz 50 MHz 49.5 MHz 56.25 MHz
1024 x 768	UVGA	8, 16, 32	60 Hz 70 Hz 75 Hz 85 Hz	48.4 kHz 56.5 kHz 60.0 kHz 68.7 kHz	65 MHz 75 MHz 78.75 MHz 94.5 MHz
1280 x 1024	SXGA	8, 16, 32	60 Hz 75 Hz 85 Hz	64 kHz 80 kHz 91.1 kHz	108 MHz 135 MHz 157.5 MHz
1600 x 1200	UXGA	8, 16, 24	60 Hz 70 Hz 75 Hz 85 Hz	75 kHz 87.5 kHz 93.8 kHz 106.3 kHz	162 MHz 189 MHz 202.5 MHz 229.5 MHz

Table 2-26 SDL Platform Display Timing Specifications (AgatePXC Only)

Active Display	Analog/ DVI	Format	Bits per Pixel	Vertical Refresh	Horizontal Refresh	Pixel Clock
640 x 480	Both	VGA	8, 16, 32	75 Hz	37.65 kHz	30.72 MHz
800 x 600	Both	SVGA	8, 16, 32	75 Hz	47.03 kHz	48.90 MHz
1024 x 768	Both	UVGA	8, 16, 32	75 Hz	60.15 kHz	81.80 MHz
1152 x 900	Analog	Sun	8, 16, 32	72 Hz	67.54 kHz	103.74 MHz
1280 x 1024	Both	SXGA	8, 16, 32	75 Hz	80.17 kHz	138.54 MHz
1600 x 1200	Analog	UXGA	8, 16, 24	75 Hz	93.98 kHz	204.49 MHz

2.14 VGA Monitor Requirements

Rastergraf boards can be used with a variety of monitors. For best performance a monitor should have the following features:

- VGA compatible 5 Wire RGB with separate TTL horizontal and vertical sync or 3 Wire RGB with sync on green (see note below)
- Switchable Termination (for monitor loopthrough)
- Height, pincushion, width, phase, and position controls
- Autotracking horizontal and vertical synchronization
- High bandwidth: 135 MHz at 1280 x 1024
  180 MHz at 1600 x 1200
- Horizontal refresh rate: 70 kHz at 1280 x 1024
  90 kHz at 1600 x 1200

Notes

In SDL (AgatePXC Only), the software defaults to standard Multiscan 5-wire RGBHV (VGA compatible) settings. If you require Sync On Green, be sure to select **SYNC ON GREEN** when setting the Video Parameters.

Some versions of the graphics boards can support interlaced operation including STANAG. Please contact Rastergraf for more information.

Composite Video Signal: 1 Volt peak to peak consisting of:
660 mV Reference White +
54 mV Reference Black +
286 mV Sync Level

Chapter 3
Front Panel Connectors and Cables

3.1 Introduction

A variety of front and rear panel connectors and related breakout cables are used on the Agate and Merlin boards. These are covered in the following sections. See Sections 1.14 and 1.15 for board part numbers and related information.

Wherever possible, the Agate and Merlin use industry standard interfaces and connectors such as VGA, USB, and DisplayPort. Nevertheless, non-standard connectors, or in some cases non-standard usage of standard connectors, have been utilized for some features.

The chapter contains the following sections:

Chapter 4 covers the PMC Pn4 and XMC Pn6 rear I/O connectors. In an effort to ease the always-problematic issues of rear I/O cabling, PIM adapters are available for both the AgatePXC and MerlinPXC (but not MerlinMTX) and these are documented in that chapter as well.

Rastergraf can supply you with some of the breakout and extension cables that are described in this chapter. Please contact Rastergraf sales for any assistance you may need.

Cable Sources

Note: Rastergraf uses an outside contractor to build its production cables:

Lynn Products, Inc. http://www.lynnprod.com

Figure 3-1 AgatePXC/2 Standard Pinout Front and Rear I/O Connections

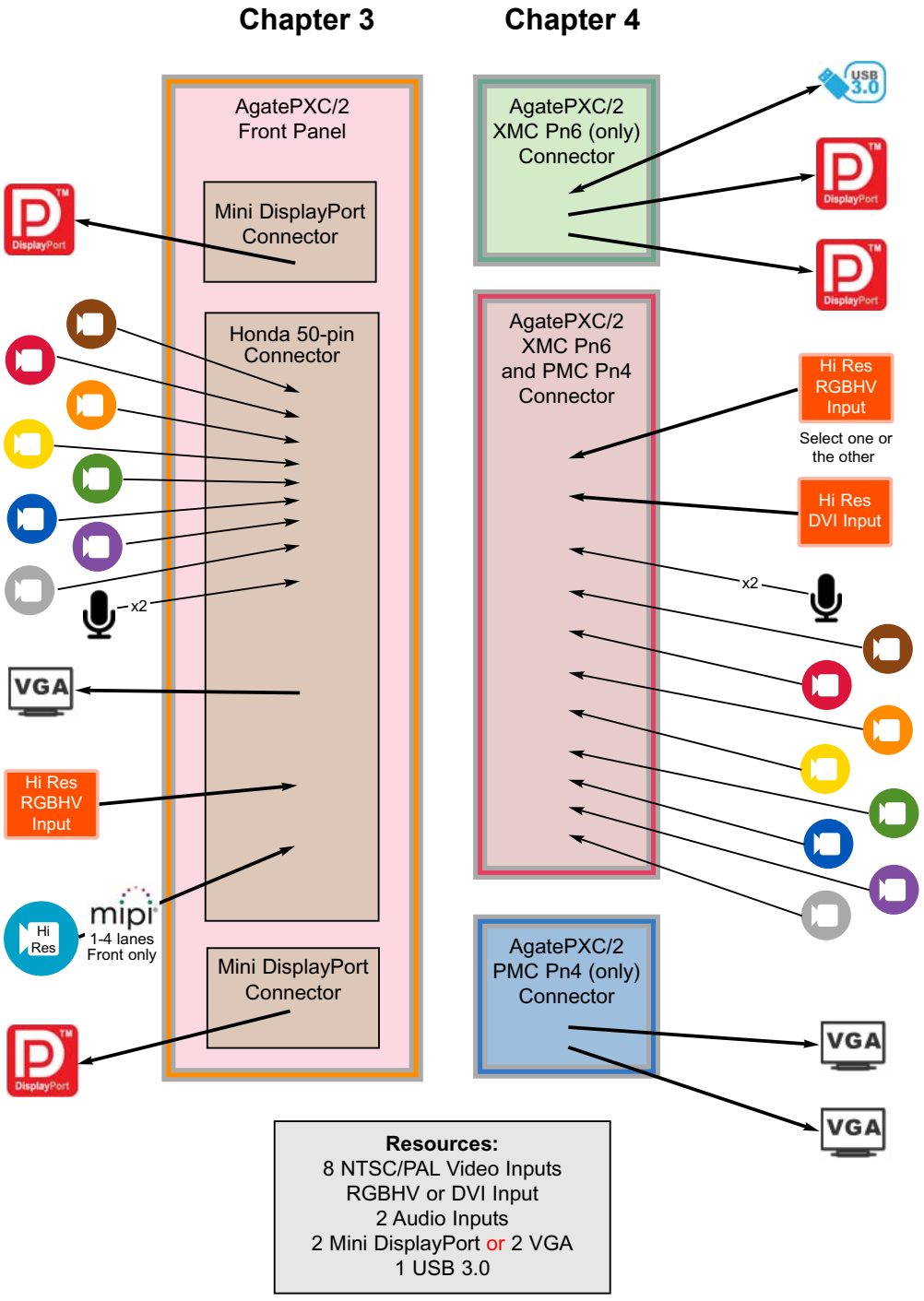


Figure 3-2 MerlinPXC/2 Standard Pinout Front and Rear I/O Connections

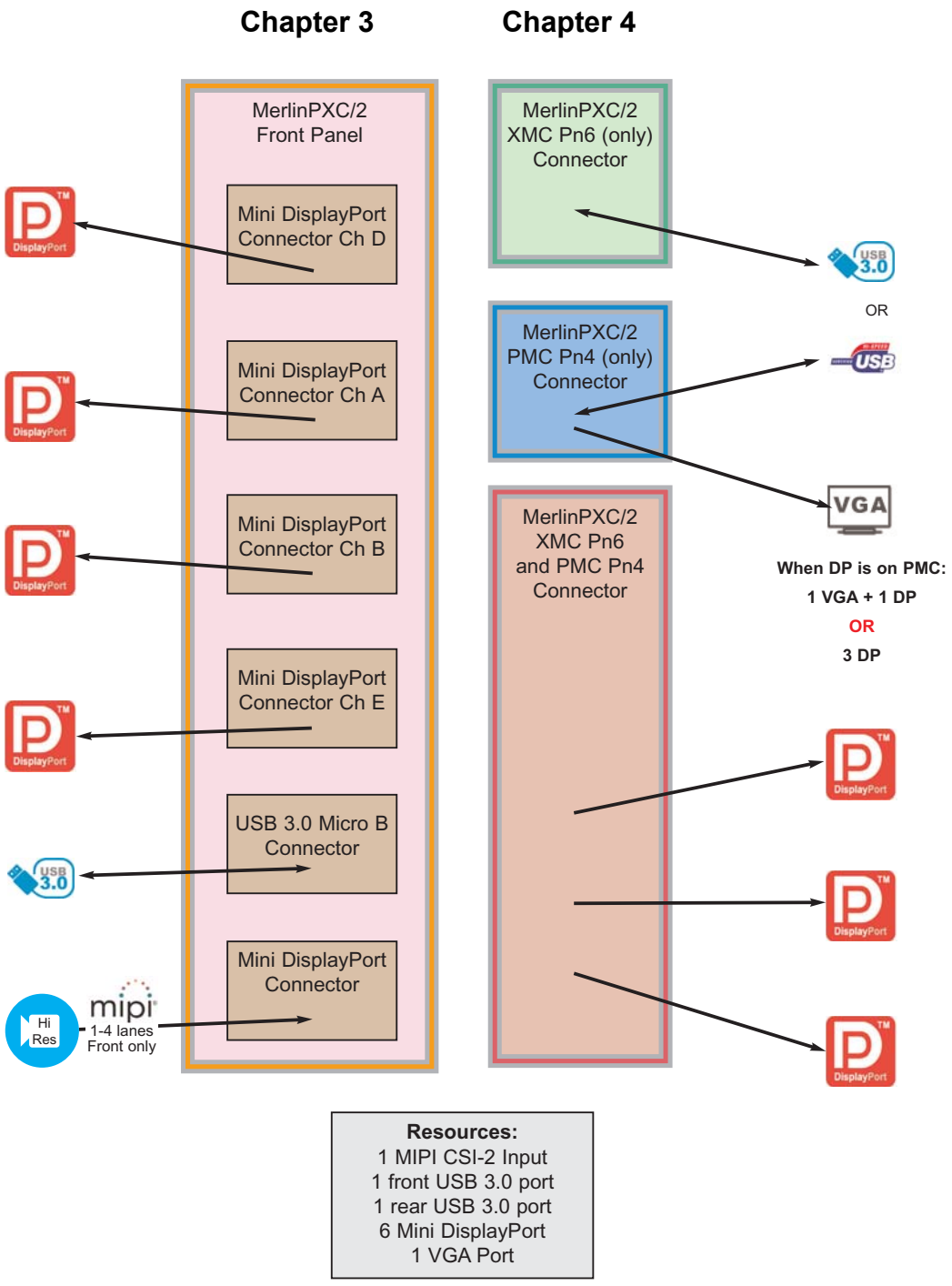
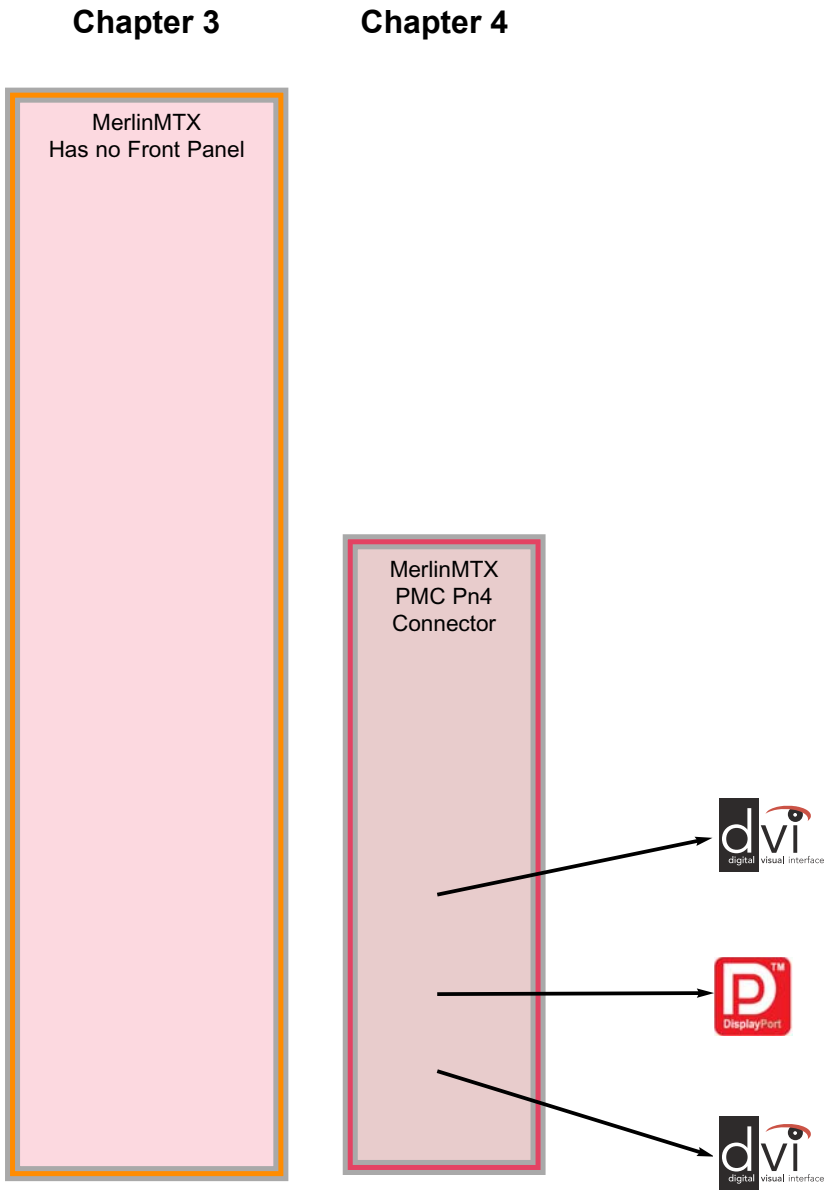


Figure 3-3 MerlinMTX Standard Pinout Front and Rear I/O Connections



3.2 VGA Connector (/1V Boards)

Analog graphics output is provided on a standard VGA style compressed 15 pin D-Sub and is used with an “Autoscan” type monitor that uses the DDC lines to determine the monitor characteristics.

You must use the correct initialization, since a VGA monitor depends on the sync polarities to determine operating frequency. The polarities of the Vertical/Composite Sync and Horizontal Sync are controlled by the Agate or Merlin graphics controller chip.

The R, G, and B video outputs are driven by the Agate or Merlin graphics controller chip which is capable of driving terminated cable (75Ω) to standard RS-330/IRE levels. Cable length should be limited to 50 feet unless you use low loss RG-59.

If you really want to roll you own, the board side VGA connector is an Kycon K31XHT-E15S-N. Be sure to use 75Ω coax for the R, G, B. You can use TP or coax on H, and V.

A cable that would work is Mogami W3206-8 or L-com.

Important Note

Because two VGA connectors are a tight fit on the AgatePXC/1V, some VGA connector moldings are too wide to allow two cables to be plugged in simultaneously. Rastergraf can supply cables that are known to fit. The cable part number is A31-00599-1012. See Section 3.8.

Figure 3-4 Typical Panel Mount VGA Connector

Figure 3-5 Panel Mount VGA Connector Pin Numbering

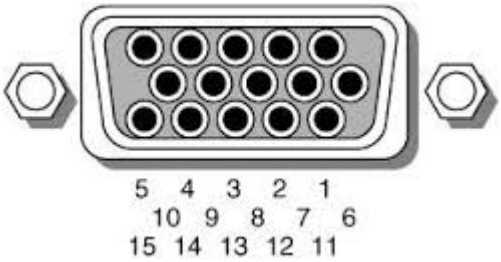


Table 3-1 Analog (VGA) Video Connector Pinout

VGA Pin	Description	Ground Type
1	Red	
2	Green	
3	Blue	
4	n/c	
5	DDC Ground	Circuit Ground
6	Red Ground	Circuit Ground
7	Green Ground	Circuit Ground
8	Blue Ground	Circuit Ground
9	Fused +5 Volts, .25A max	
10	Sync Ground	Circuit Ground
11	Ground	Circuit Ground
12	DDCDA	
13	HSYNC	
14	VSYNC	
15	DDCCK	
-	Connector Shell	Chassis Ground
-	Outer Shield (Cable Jacket)	Chassis Ground

Warning:

The Chassis Ground **MUST NOT BE CONNECTED** to Circuit Ground.

3.3 Mini DisplayPort Connector (/2 or /1D Boards)

Both the Agate and Merlin support DisplayPort using the industry standard Mini DisplayPort connector. DisplayPort uses 100 Ω shielded twisted-pair, length-matched cables for the all five differential signal pairs.

See https://en.wikipedia.org/wiki/Mini DisplayPort for more information. Note that DisplayPort works with in-line-cable dongles that can convert the DP signal to DVI, HDMI, VGA, or LVDS. With Merlin's DisplayPort 2.0, you can run several monitors on one port.

Figure 3-6 Typical Panel Mount Mini DisplayPort Connector

Table 3-2 Mini DisplayPort

Mini DisplayPort Pin	Description
1, 7, 8, 13, 14, 19	GND
21, 22, 23, 24	GND_CHASSIS
3	MDPx0P
5	MDPx0N
9	MDPx1P
11	MDPx1N
15	MDPx2P
17	MDPx2N
10	MDPx3P
12	MDPx3N
16	MDPx_AUXP
18	MDPx_AUXN
2	MDPx_HPD
4	MDPx_PIN13
6	MDPx_CEC
20	PDPx_PWR

3.4 LVDS Connector (AgatePXC/1L)

The AgatePXC/1L provides a front panel Mini Camera Link (MCL) pinout compatible Honda SDR26 connector. See Section 1.12.2.2 for more information. The pinout follows the MCL configuration for the sake of convenience of cable availability - there is NO support for Camera Link on the AgatePXC/1L. LVDS uses 100 Ω shielded twisted-pair, length-matched cable. All 10 differential pairs must be the same length.

Figure 3-7 Typical SDR26 LVDS Connector

Table 3-3 LVDS Front Panel Connector (AgatePXC/1L)

SDR26 Pin	Signal Name
1, 26	reserved
13, 14	Ground
2	R_LVDS_U3P
15	R_LVDS_U3N
3	R_LVDS_U2P
16	R_LVDS_U2N
4	R_LVDS_U1P
17	R_LVDS_U1N
5	R_LVDS_U0P
18	R_LVDS_U0N
6	R_LVDS_U0CP
19	R_LVDS_U0CN
7	R_LVDS_U3P
20	R_LVDS_U3N
8	R_LVDS_U2P
21	R_LVDS_U2N
9	R_LVDS_U1P
22	R_LVDS_U1N
10	R_LVDS_U0P
23	R_LVDS_U0N
11	R_LVDS_U0CP
24	R_LVDS_U0CN
12	R_LVDS_DIGON
25	R_LVDS_VARY_BL

3.5 USB Connector (MerlinPXC/2)

The USB 3.0 SuperSpeed port is able to support up to 5Gbps data rate, as compared to the older USB 2.0, which supports up to 480Mbps. See Section 1.10 for information about the uPD720101 USB Host Controller.

It should be pointed out that while USB 3.1 has now been released, the Merlin and Agate support USB 3.0. While some of the enhancements in USB 3.1 are oriented to make USB more consumer friendly, there are some other, interesting possibilities with USB 3.1 for future products. In any case, neither a USB 3.1 host controller nor even connectors were ready in time for implementation on either the Agate or Merlin.

This section just covers the front panel USB connector for the Merlin. Since the Agate only has USB on the rear I/O connector, that and the Merlin's rear USB connection are covered in Chapter 4.

The Merlin front panel connector uses a USB 3.0 Micro AB connector (Kycon KMMX-AB10-SMT1SB30TR).

Figure 3-8 Kycon USB 3.0 Micro AB Connector

Table 3-4 MerlinPXC/2 USB Connector - USB 3.0 Type Micro AB

USB Pin	Name
1	Switched Power (3.3V)
2	USB 2.0 Data –
3	USB 2.0 Data+
4	ID (n/c)
5	Power Ground
6	USB 3.0 SS_TX-
7	USB 3.0 SS_TX+
8	SS_Ground_Drain
9	USB 3.0 SS_RX-
10	USB 3.0 SS_RX+

3.6 MIPI Connector (MerlinPXC/2)

The Merlin uses a Mini DisplayPort connector for the MIPI CSI-2 input for convenience. There is no standard MIPI connector. One reason for this is perhaps because traditionally, the MIPI cameras are used in embedded, dedicated applications such as cell phones. MIPI cameras are very high resolution, fast, inexpensive, and readily available, making them attractive for many applications.

Although the typical MIPI cable length is specified at 30cm or so, experiment has shown that they are good for much longer, no doubt because they use the tried and true LVDS signal technology.

Just as with any LVDS application, the MIPI CSI-2 uses 100 Ω shielded twisted-pair, length-matched cables for the all five differential signal pairs.

Table 3-5 MerlinPXC/2 MIPI CSI-2 Input Connector

Mini Display Pin	Description
1, 7, 8, 13, 14, 19	GND
21, 22, 23, 24	GND_CHASSIS
3	MIPI_D0P
5	MIPI_D0N
9	MIPI_D1P
11	MIPI_D1N
15	MIPI_D2P
17	MIPI_D2N
10	MIPI_D3P
12	MIPI_D3N
16	MIPI_CKP
18	MIPI_CKN
2	Not used
4	XMIP_SCL
6	XMIP_SDA
20	MIPI_VDD

3.7 DVI Input Connector (AgatePXC/2)

It is suggested that you use a DVI-D connector for breaking out the DVI ***input*** from the Agate PMC Pn4 backplane connector. This will make it easy to connect to any DVI source.

Just to clarify, neither the AgatePXC nor MerlinPXC directly support DVI ***out.*** You have to use external DisplayPort to DVI dongles. See Section 3.13. On the other hand, the MerlinMTX DOES support DVI Out, but only on the PMC Pn4 connector.

See Sections 4.10 and 4.11 for a wirelists using the DVI-D connector.

The industry standard DVI-D (digital only) connector carries just the DVI digital graphics signals. See http://www.ddwg.org/ for more information.

The DVI protocol uses the TMDS encoded data format. Each of the three differential data pairs encodes nine digital video (TTL) signals. A separate pair carries the clock. DVI requires all pairs be closely matched in length.

Each data pair must be 100 Ω shielded twisted-pair, and must be length-matched for the all four differential signal pairs.

Table 3-6 AgatePXC/2 Rear I/O DVI-D Connector

DVI-I Pin	Description
1	DVI_TX2L
2	DVI_TX2H
3	DVI_TX2 Shield/Ground
9	DVI_TX1L
10	DVI_TX1H
11	DVI_TX1 Shield/Ground
17	DVI_TX0L
18	DVI_TX0H
19	DVI_TX0 Shield/Ground
22	DVI_TXC Shield/Ground
23	DVI_TXCH
24	DVI_TXCL

3.8 DVI-I Connector (MerlinMTX)

The MerlinMTX supports DVI on its PMC Pn4 rear I/O connector. The MerlinMTX PIM passes the DVI connections through, but uses the DVI-I (analog/digital) version which carries both the DVI digital and the VGA analog signals. In the case of the MerlinMTX, however, the VGA pins are used to pass video in or audio in signal.

An additional cable assembly converting the VGA connection to separate BNC connectors, such as that found in Section 3.11.4, can be used to connect to the audio and video input signals.

Table 3-7 DVI-I Connector as used on MerlinMTX PIM

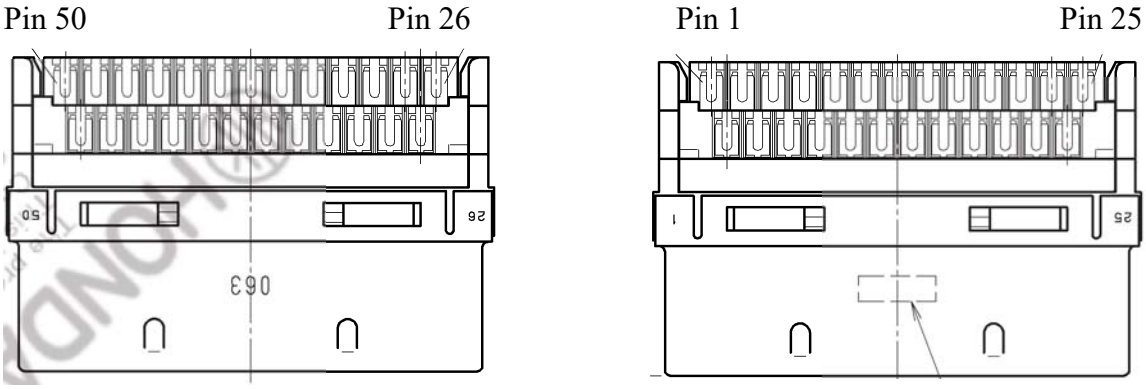
DVI-I Pin	Description
1	DVI_TX2L
2	DVI_TX2H
3	DVI_TX2 Shield/Ground
6	DDCCK
7	DDCDA
8	n/c (VS)
9	DVI_TX1L
10	DVI_TX1H
11	DVI_TX1 Shield/Ground
14	Fused +5 Volts, .25A max
15	Ground
17	DVI_TX0L
18	DVI_TX0H
19	DVI_TX0 Shield/Ground
22	DVI_TXC Shield/Ground
23	DVI_TXCH
24	DVI_TXCL
4, 5, 12, 13, 16, 20, 21	n/c
C1	AIN8 or VIN8 (Red)
C2	VIN1 (Green)
C3	VIN2 (Blue)
C4	AIN8 or VIN8 (HS)
C5	Analog Ground

3.9 Multi-Function I/O Connector (AgatePXC/2)

The AgatePXC/2 has a front panel Honda SDR50 (HDR-EC50LFDT+) I/O connector that supports 2 different pinout option: 50A and 50B. The latter is available only by special order.

Figure 3-9 Typical SDR50 Connector

Mating connector: HDR-E50MSG1+ and HDR-E50LPH shell - see onlinecomponents



Cable sets follow connector pin arrangement: twisted wire pair plus ground. Use this arrangement to get even length of wire pairs through the connector

3.9.1 Pinout 50A: Out: VGA; In: MIPI, 2x Audio, 8x NTSC/PAL, RGBHV

The ***Pinout 50A*** supports the standard configuration of the AgatePXC/2. It includes a 8 NTSC/PAL video inputs, 2 audio inputs, an RGBHV input, the Ch 2 VGA output, and a 4-lane MIPI CSI-2 port.

If you look ahead to the Pinout Table, you will see that the pins are listed according to their intended grounds. If you plan to build your own cable, please follow this arrangement.

Rastergraf has a breakout cable that expands the 50-pin SDR connector out into standard connectors. See Section 3.10.

3.9.1.1 8x NTSC/PAL Inputs

VIN1-VIN8 are composite NTSC/PAL Inputs. Each input is connected to the CX25858 digitizer by a 1.0 uF input capacitor and presents a (DC) 75Ω impedance to the driving source. No low pass filtering is done on the signals. Each VINx has its own A to D converter and DMA transfer engine, which allows all 8 channels to be acquired at the same time. The cabling should use 75Ω coax.

VIN Loopback Mode

As a test feature, a control bit can make the E4690 VGA Ch 2 COMP output loopback to VIN8. The only time the loopback should be enabled is when VIN8 is not otherwise connected. Also, of course, E4690 VGA Ch 2 must be programmed for TV Out mode.

3.9.1.2 2x Audio Inputs

AIN7 and AIN8 are audio inputs configured as a stereo pair. AIN 7/8 were chosen because that is the default pair in the Conexant Windows driver.

Both inputs are connected to the CX25858 digitizer by a 2.2 uF input capacitor and present a high impedance of about 180KΩ at 500Hz to the driving source. No low pass filtering is done. They each have their own A to D converter and DMA transfer engine, which allows both channels to be acquired at one time. The cabling should use 50Ω coax.

3.9.1.3 RGBHV Input

The I/O connector can be used to connect to the high-speed RGBHV digitizer which uses the ADV7441A/FX3 combination to acquire RGBHV or RGB + SOG, up to 1600 x 1200 at 160 MHz.

The RGB inputs are connected through front-end Murata NFL21SP107 100 MHz low-pass filters and then to the ADV7441A by a 0.1 uF input capacitor. They present a (DC) 75Ω impedance to the driving source. The cabling should use 75Ω coax.

The output of the ADV7441A is linked to a FX3 USB SuperSpeed peripheral controller which uses the standard USB UVC software protocol to transfer acquired video data to the host.

3.9.1.4 VGA Ch 2 Output

The AgatePXC/2 has 2 Mini DisplayPort connectors on the front panel and no room for VGA. In some cases, it may be convenient to have VGA, so Pinout 50A provides it. Remember that you still can only have 2 active display channels at one time. The R, G, B, H and V cabling should use 75Ω coax, and the DDC lines should use twisted pair with ground.

3.9.1.5 MIPI CSI-2 Input

The Agate MIPI port supports 1-4 lanes MIPI CSI-2 compatible devices. The port is connected directly to a CX3 USB SuperSpeed MIPI controller which uses the standard USB UVC software protocol to transfer acquired video data to the host.

The MIPI CSI-2 signal pairs cabling should use 100Ω, shielded twisted-pair, length-matched cables for the all differential signal pairs. If you construct your own cables be sure to use an approved cable vendor and make sure that the wiring is very clean and properly length-matched. Unlike DisplayPort or PCIe, all 5 differential pairs must be the same length as each other.

See Section 3.14 for notes about building your own MIPI cabling and about the WandCam adapter boardlet.

Note: a board stuffing option selects voltage to be 1.8V or 3.3V for MIPI I^2C port. The default is 3.3V.

3.9.1.6 Suggested Cabling Sources

A micro-miniature 75Ω coax cable source:

Whitmor W-4769-4478 OD = 0.047 in

A micro-miniature 50Ω coax cable source:

Whitmor W-4269-3254 OD = 0.029 in

The best thing is to contact Lynn Products. They have built our custom cables for years.

Table 3-8 AgatePXC/2 Multi-function I/O Connector Pinout 50A

	SDR Pin	Standard Pinout (50A)	SDR Pin	Standard Pinout (50A)	
	1	MIPI_D3N	26	MIPI_D1N	
	2	MIPI_CKN	27	MIPI_D0N	
	3	MIPI_D3P	28	MIPI_D1P	
	4	MIPI_CKP	29	MIPI_D0P	
	5	GND	30	GND	
	6	GND	31	GND	
	7	MIPI_D2N	32	XMIP_SDA	
	8	FP_HS_C_IN	33	FP_PWR	
	9	MIPI_D2N	34	XMIP_SCL	
	10	GND	35	GND	
	11	GND	36	FP_R_IN	
	12	FP_VS_IN	37	FP_G_IN	
Default = VS2	13	FP_NC_**VS2**	38	FP_B_IN	
	14	FP_VIN4	39	FP_VIN8	
	15	FP_VIN2	40	FP_VIN6	
	16	GND	41	GND	
	17	GND	42	GND	
	18	FP_VIN3	43	FP_VIN7	
	19	FP_VIN1	44	FP_VIN5	
Default = CR2	20	FP_AIN4_**CR2**	45	FP_VIN8	
Default = DA2*	21	FP_AIN2_**DA2**	46	FP_AIN6_**HS2**	Default = HS2
	22	GND	47	GND	
	23	GND	48	GND	
Default = MB2	24	FP_AIN3_**MB2**	49	FP_AIN7	
Default = DC2*	25	FP_AIN1_**DC2**	50	FP_AIN5_**YG2**	Default = YG2

* Note – this is not included on Agate Rev 1.

3.9.2 Pinout 50B: MIPI, 8x Audio, 8x NTSC/PAL, RGBHV

Pinout 50B is a special build version to be requested at order time.

Table 3-9 AgatePXC/2 Multi-function I/O Connector Pinout 50B

	SDR Pin	Optional Pinout (50B)	SDR Pin	Optional Pinout (50B)	
	1	MIPI_D3N	26	MIPI_D1N	
	2	MIPI_CKN	27	MIPI_D0N	
	3	MIPI_D3P	28	MIPI_D1P	
	4	MIPI_CKP	29	MIPI_D0P	
	5	GND	30	GND	
	6	GND	31	GND	
	7	MIPI_D2N	32	XMIP_SDA	
	8	FP_HS_C_IN	33	FP_PWR	
	9	MIPI_D2N	34	XMIP_SCL	
	10	GND	35	GND	
	11	GND	36	FP_R_IN	
	12	FP_VS_IN	37	FP_G_IN	
Default = NC	13	FP_**NC**_VS2	38	FP_B_IN	
	14	FP_VIN4	39	FP_VIN8	
	15	FP_VIN2	40	FP_VIN6	
	16	GND	41	GND	
	17	GND	42	GND	
	18	FP_VIN3	43	FP_VIN7	
	19	FP_VIN1	44	FP_VIN5	
Default = AIN4	20	FP_**AIN4**_CR2	45	FP_VIN8	
Default = AIN2*	21	FP_**AIN2**_DA2	46	FP_**AIN6**_HS2	Default = AIN6
	22	GND	47	GND	
	23	GND	48	GND	
Default = AIN3	24	FP_**AIN3**_MB2	49	FP_AIN7	
Default = AIN1*	25	FP_**AIN1**_DC2	50	FP_**AIN5**_YG2	Default = AIN5

* Note – this is not included on Agate Rev 1.

3.10 Development Connectors

There are two connectors used for accessing STM32F427 functions. In addition, there are 3-pin headers for accessing the CX3 and FX3 UART ports.

Figure 3-10 AgatePXC LED and Development Connector Locations

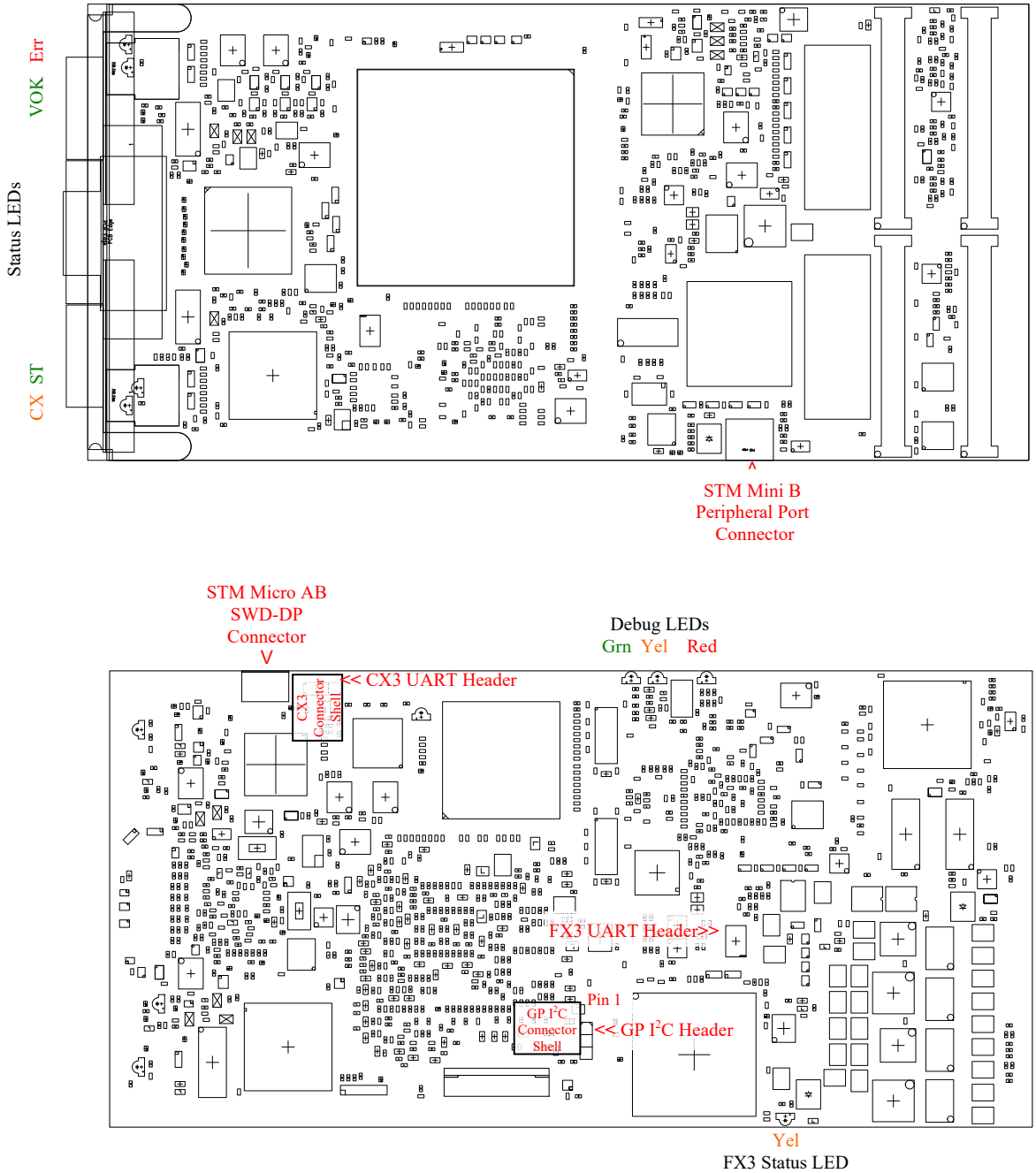


Figure 3-11 MerlinPXC Development Connector Locations

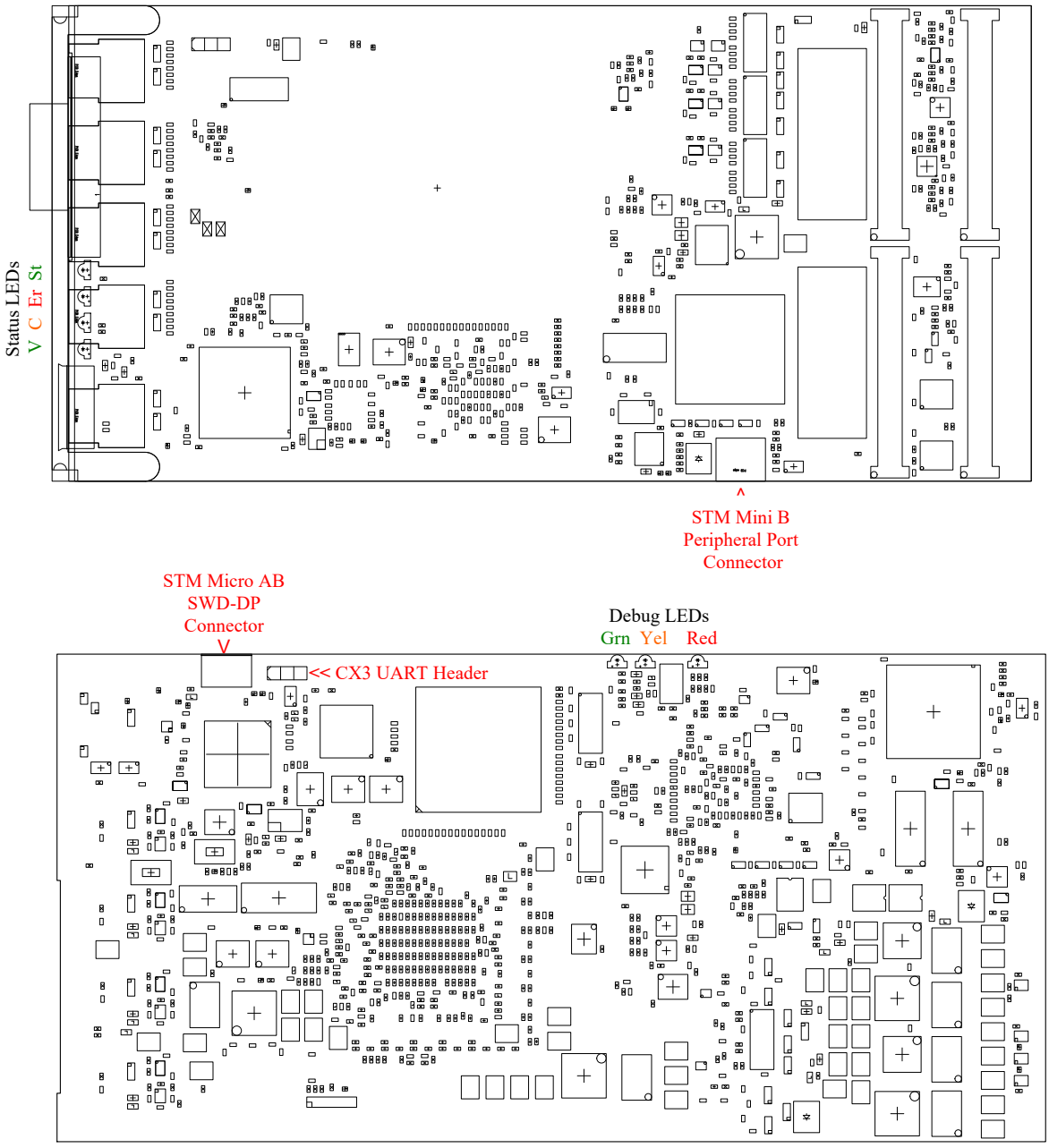
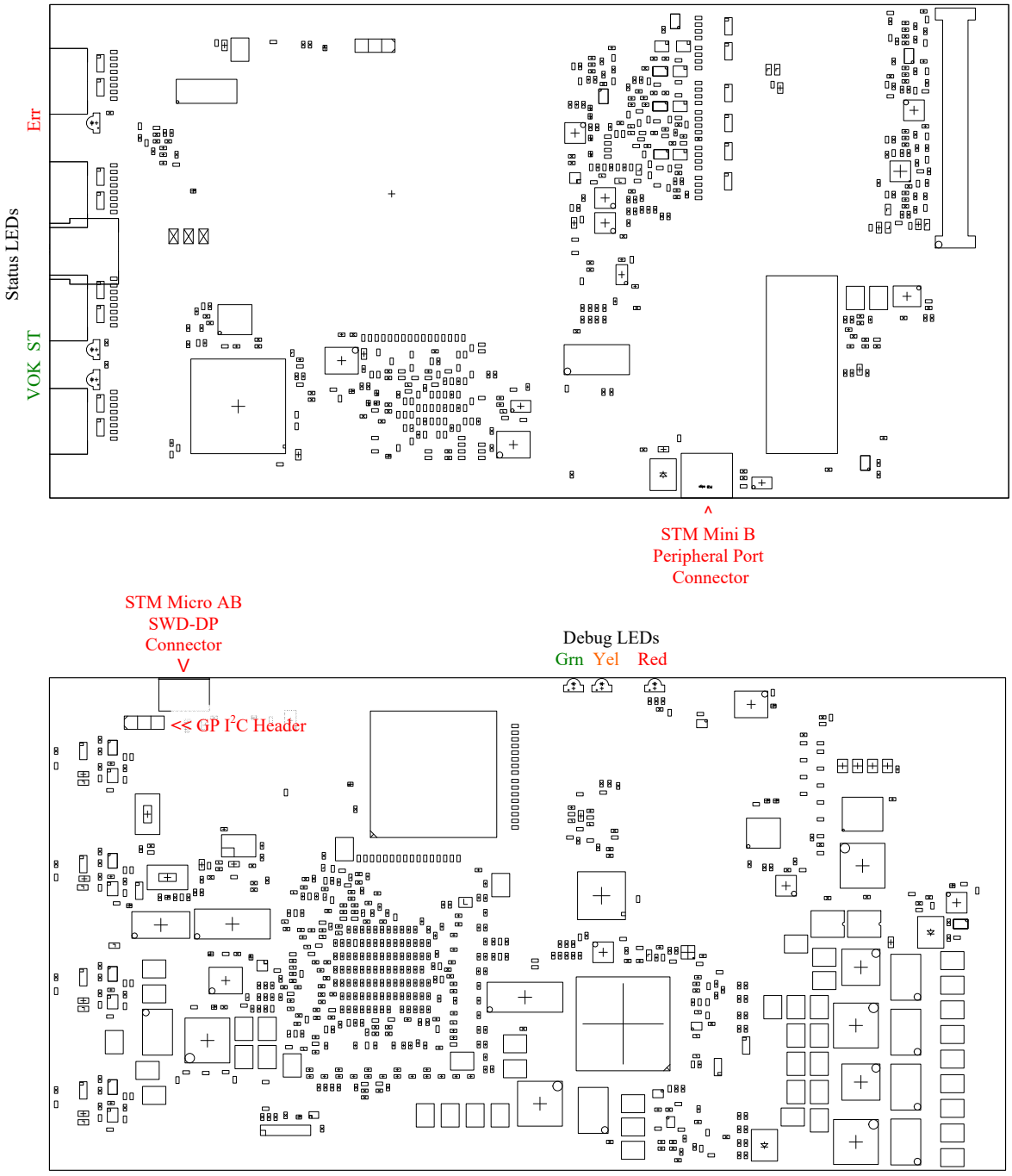


Figure 3-12 MerlinMTX Development Connector Locations



3.10.1 STM SWD-DP Debug Port Connector (Agate/Merlin)

This port is not intended for the general use. It is used to gain debugger access to the STM32F427 for firmware update or tinkering.

In order to use the port, you have to order an ST-LINK/V2. Also, you have to build the cable that connects the ST-LINK/V2 to J012C6.

Figure 3-13 ST-LINK/V2 Debugger Pod

J012C6 provides access to the Agate or Merlin STM32F427 **SWD-DP** debug port, which uses a 2-pin (clock and data) interface based on the ARM Serial Wire Debug (SWD) protocol.

J012C6 is located on Side 2 of the PCB, which is exposed when the board is installed, near the front panel. Depending on your system setup, this may not be the most convenient location, but neither the front panel nor the rear I/O ends of the board were an option.

For convenience, J012C6 uses a USB 2.0 Micro AB connector (JAE DX4R205JJAR1800) but **IS NOT A USB PORT.**

A short cable from J012C6 links to the ST-LINK/V2 in-circuit debugger/programmer, whose other port connects to a PC USB port.

To build the cable, obtain a USB Micro B M-F extension cable that is known to be 5-wire cable like this one or this one. The cable **MUST** have all 5 wires connector to connector. M/F extension cables are the best bet.

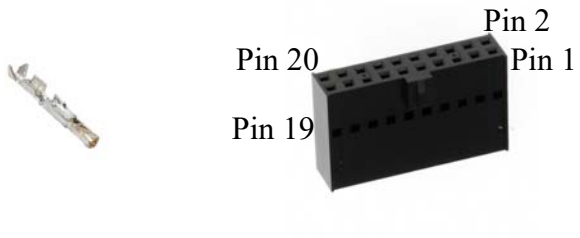
Figure 3-14 Typical USB Micro B M/F Extension Cable

Then, from Digikey, obtain the housing and at least 10 pins:

Harwin: M20-1071000 connector shell

Harwin: M20-1180042 pins

Figure 3-15 20-pin 0.1" 2x10 Housing and Pin



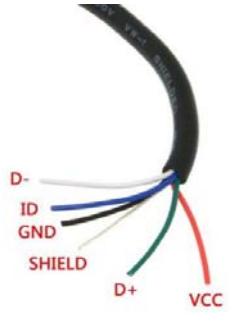
Map (showing the end of shell where you insert pins/wires

2	4	6	8	10	12	14	16	18	20
1	3	5	7	9	11	13	15	17	19

^ ++++++++++ << polarizer notch on
Pin 1 ST-Link/V2 pin 1
indicator

Table 3-10 Wirelist for SWD Cable and Cable End Breakout

Micro USB Cable Pin	USB Cable Name	USB Cable Color Std	USB Cable Color L-Com	Molex Housing Pin	Agate/ Merlin Signal Name
1	Switched Power	Red	Red	1	SWD VDD
2	Data –	White	White	7	STM_DIO
3	Data+	Green	Green	15	SW_RSTL
4	ID	Blue	Black	9	STM_CLK
5	Ground	Black	Yellow	18	Ground
-	Ground	Shield	Shield	20	Ground



You will need to download and install some software for the ST-LINK/V2. Section 8.9 has some useful information about what you can do with this port and to use it.

3.10.2 STM Mini B Peripheral Port Connector (Agate/Merlin)

3.10.2.1 Introduction

The STM32F427 (’427) has two USB OTG ports: the High Speed Port (OTG_HS) and the Full Speed Port (OTG_FS).

In general, the ports are interchangeable in terms of functions except for one crucial difference. When the ’427 BOOTx start-up jumpers are set correctly, the OTG_FS port is used by the internal boot loader to auto-load the application firmware (DFU mode). With this feature, an external memory-stick could serve as a convenient update source.

The alternative to using the boot loader is to use the SWD-DP (see Section 3.8.1) and run the debugger software to download a new image.

Jumpers on the AgatePXC or MerlinPXC board enable the STM Peripheral Port Connector to be connected to either port. Please see Section 5.4.2 for information about setting the OTG_HS/OTG_FS jumpers and Section 5.4.1 SW9 about the BOOT0 settings.

The MerlinMTX connector is hardwired to the FS port.

By default, both the AgatePXC and MerlinPXC are shipped with the FS port jumpers set for the connector.

Please refer to Section 1.13 for a description of the ISM features.

Please refer to Section 6.3 for information about how to use the ISM.

Please refer to Section 8.9 for information about the software needed to connect to the ISM.

3.10.2.2 Standard Use of the Connector - ISM

In most cases, you want to just access the ISM firmware that is preloaded into the STM32F427. The Mini B (J011D5) connector is located on Side 1 of the PCB (covered when the board is installed). For location, please see Figure 3-10 for the AgatePXC, Figure 3-11 for the MerlinPXC, and Figure 3-12 for the MerlinMTX.

By default, the MerlinPXC is shipped with the FS port jumpers set for ISM use. **The MerlinMTX Mini B connector is hardwired to FS.** The ISM firmware that has been preloaded uses the FS port.

Note that you have to download a new version of ISM to use the HS port and that has to be done via the SWD-DP port (see previous page).

3.10.2.3 Non-Standard Use of the Connector

Using the SWD-DP debugger connector, you can overwrite the ISM firmware and do what you will with STM32F427. Of course, we can’t support you on this except to tell you what is connected and how.

3.10.3 CX3 UART Access (AgatePXC/MerlinPXC)

The Cypress CX3 MIPI SuperSpeed Controller is normally accessed via its USB port and can be downloaded via an on-board uPD720201 USB host port with code supplied by the operating system.

The best way to debug the CX3 is via its JTAG port and debugger system. However, the CX3 JTAG port is linked into the board JTAG loop, and for a variety of reasons, it wasn't practical to provide access to it.

As a fallback, access the CX3's UART port has been provided. This port can be used as a debugging tool although not with the same control as the JTAG port would provide. It would be used by putting print statements in the code and, possibly, awaiting input.

Please see Section 3.9.6 for instructions on how to install the header on the board.

You do need a TTL to RS-232 converter, since the UART signals that the CX3 supplies are TTL. A good converter is this:

Figure 3-16 Olimex MOD-RS232

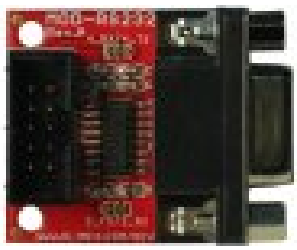


Table 3-11 CX3 UART 2mm Header (JP012C6)

JP012C6 Header Pin	Signal to CX3 Port	MOD-RS232 2x5 0.1" Header
1	CX3_UART_TX	3
2	GND	2
3	CX3_UART_RX	4
*	VDD	1

* The VDD pin was inadvertently omitted from the JP012C6 header. Please contact Rastergraf for assistance in locating a convenient place to pick up VDD on the board.

3.10.4 FX3 UART Access (AgatePXC)

The Cypress FX3 SuperSpeed Peripheral Controller is normally accessed via its USB port and can be downloaded via an on-board uPD720201 USB host port with code supplied by the operating system.

The best way to debug the FX3 is via its JTAG port and debugger system. However, the FX3 JTAG port is linked into the board JTAG loop, and for a variety of reasons, it wasn't practical to provide access to it.

As a fallback, access the FX3's UART port has been provided. This port can be used as a debugging tool although not with the same control as the JTAG port would provide. It would be used by putting print statements in the code and, possibly, awaiting input.

The FX3 UART pins are shared with the FX3 boot PROM SI and SO pins. The PROM is ordinarily not used, since the FX3 will boot from the OS. It is only used in the case that there are problems with the autoboot process.

If you do want to use the UART function, JP012J3 and 0-ohm RP021H2 have to be installed and then you will need to make a small cable.

JP012J3 is a 2x4 0.50" header, Major League Electronics LTSHSM-504-D-04-F-V-LF or Samtec FTS-104-02-F-DV.

Although it is possible to get a mating connector housing and pins ***we recommend that you do NOT do this***.

It will put a lot of leverage on the JP012J3, which is a surface mount connector (there wasn't room for a 2mm through-hole connector), and the header is very likely to get torn off. Instead, use micro EZ hooks to connect between the header pins and a pigtail ribbon cable to the TTL to RS-232 adapter (same as CX3 – see Section 3.6.3).

Table 3-12 FX3 UART 0.50" Header (JP012J3)

JP012J3 Header Pin	Signal to FX3 Port	MOD-RS232 2x5 0.1" Header
4	FX3_UART_TX	3
5	GND	2
1	FX3_UART_RX	4
*	VDD	1

* The VDD pin was inadvertently omitted from the JP012J3 header. Please contact Rastergraf for assistance in locating a convenient place to pick up VDD on the board.

3.10.5 GP I²C Access Header (AgatePXC/MerlinMTX)

The STM processor accesses the on-board devices via a two-wire I²C bus called GP_ I²C. Access to this bus is shared with control bits on the 24T6 so that host based software can also access these devices.

Because this 24T6 access uses programmed I/O bits rather than a real I²C bus, handshaking has to be done between the STM and the host controlling the 24T6 bits in order to avoid a conflict, since programmed I/O bits can't resolve an I²C multi-master collision. Please see Section 5.7 for information regarding the handshaking and the 24T6 control bits.

Please see Section 3.9.6 for instructions on how to install the header on the board.

Note that this header is not available on the MerlinPXC.

Pin List:

Pin 1 (pin farthest from the edge of the board): GP_SDA

Pin 2 (middle pin): GP_SCL

Pin 3 (pin closest to the edge of the board): Ground

Table 3-13 GP I²C 2mm Header (JP012G2)

JP012G2 Header Pin	Signal Name
1	GP_SDA
2	GP_SCL
3	GND

3.10.6 Installing a 3-pin Header at JP012G2 or JP012C6

Referring to Figure 3-9 (AgatePXC) or 3-10 (MerlinPXC), an optional 2mm 3-pin header can be installed at the I^2C header (JP012G2, AgatePXC or MerlinMTX) or the CX3 header (JP012C6 header, AgatePXC or MerlinPXC).

There is a little trick to installing the header.

a) the header will be mounted on Side 2 of the PCB

b) please orient the header such that the pins that are bent coming out of the header plastic frame are pointing to the front panel end of the board;

c) mount the header such that pins that come straight out of the plastic frame are inserted into the header holes on Side 2 of the PCB;

d) solder the pins of the header on Side 1

This mounting method is backwards from how you might expect to install the header but is it done this way to ensure that the header pins sit far enough above the components on Side 2 so that you can plug the mating connector in.

If you put the header in the “right way”, the header pins will only be about 1mm off the PCB and that isn’t enough for the mating connector to clear the other parts in the area.

The pins will sit at about 3mm above the PCB, which should be safe and not run the risk of contacting an adjacent board. If you are unsure, CHECK!!!

Connector parts required to build a cable:

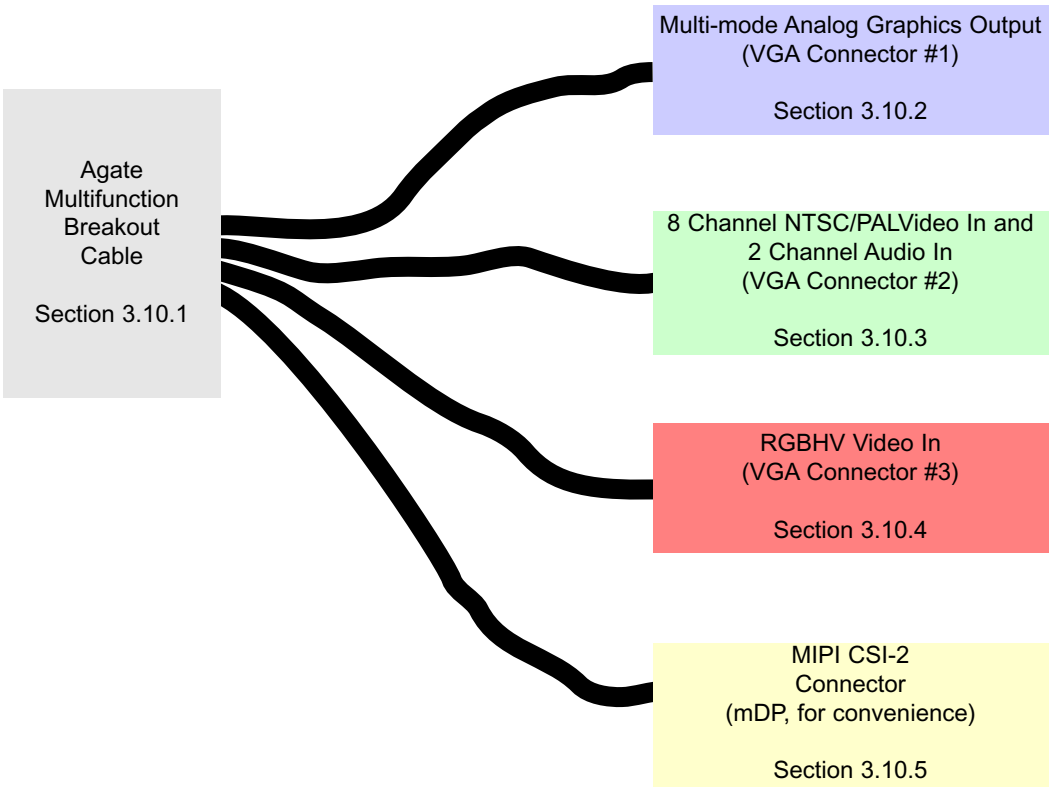
3-pin vertical header:	Harwin: M22-2510305	Digikey: 952-1312-ND
Mating connector shell:	Harwin: M22-3010300	Digikey: 952-1324-ND
Crimp pins:	Harwin: M22-3050042	Digikey: 952-1337-ND

Pins can accept 24-30 ga wire

3.11 Multi-Function Breakout Cable (AgatePXC/2)

The Agate 50-pin Multifunction cable enables access most of the AgatePXC/2's I/O functions. See Section 3.4 for more information.

Figure 3-17 Agate Multifunction Breakout Cable (mockup)



3.11.1 Board Side Connector

The board side connector is a Honda SDR50 (HDR-E50MSG1+). For pinout information, see Section 3.8.

3.11.2 Multi-mode Analog Graphics Output Connector

This is nothing more than VGA Channel 2. It is called Multi-mode because the output can be driven by the E4690 TV Encoder instead of the standard graphics output. In addition to NTSC/PAL, it can also support a variety of HD and component TV formats.

You must have the AgatePXC/2 configured for Pinout 50A to have access to the function.

Of course, the connector is just a standard board-side VGA.

Table 3-14 Multi-mode Analog Graphics Output Connector

Agate Breakout Cable VGA #1 Connector Pin	Wire Type	Description
1	75 coax #R	Red
2	75 coax #G	Green
3	75 coax #B	Blue
5	TP+S #SC/A	DDC Ground
6	75 coax #R	Red Ground
7	75 coax #G	Green Ground
8	75 coax #B	Blue Ground
9	straight	F3.3V
10	75 coax #H	HS Ground
11	75 coax #V	VS Ground
12	TP+S #SA	SDA
13	75 coax #H	HS
14	75 coax #V	VS
15	TP+S #SC	SCL

Note: yes, the voltage out for VGA is only 3.3V on this connector and that may not be adequate for some applications. You may have to supply 5V externally.

3.11.3 NTSC/PAL Video and Audio Input Connector

For convenience, the NTSC/PAL and Audio connector uses a VGA connector. It may seem a bit useless to provide a cable end that doesn't have BNCs on it, but experience has shown that users require a variety of lengths and connections. You can build your own cable to fit your needs or obtain a VGA to 8 video + 4 audio (2 audios are not used) cable here:

Figure 3-18 Example of a VGA to RGBHV Breakout Cable

Table 3-15 NTSC/PAL Video and Audio Input Connector

Agate Breakout Cable VGA #2 Connector Pin	Wire Type	Description
1	75 coax	Video 6
2	75 coax	Video 5
3	75 coax	Video 4
4	75 coax	Video 3
5	75 coax	Video 2
6	75 coax	Video 8
7	75 coax	Video 7
8, 9, shell	shields	Ground
10	75 coax	Video 1
11	50 coax	Audio 1
12	50 coax	Audio 2
13	shields	Ground
14	n/c	Not used
15	n/c	Not used

3.11.4 RGBHV Input Connector

For convenience, the RGBHV connector uses a VGA connector. It may seem a bit useless to provide a cable end that doesn't have BNCs on it, but experience has shown that users require a variety of different length RGBHV. Since VGA to RGBHV cables of a various lengths are readily available it makes sense to do it this way. You can build your own cable or obtain a cable like this:

Figure 3-19 Example of a VGA to RGBHV Breakout Cable

Table 3-16 RGBHV VGA-style Connector

Agate Breakout Cable VGA #3 Connector Pin	Wire Type	Description
1	75 coax #R	Red
2	75 coax #G	Green
3	75 coax #B	Blue
6	75 coax #R	Red Ground
7	75 coax #G	Green Ground
8	75 coax #B	Blue Ground
10	75 coax #H	HS Ground
11	75 coax #V	VS Ground
13	75 coax #H	HS
14	75 coax #V	VS

3.11.5 MIPI CSI-2 Camera Connector

Rastergraf uses a Mini DisplayPort (mDP) connector because there isn't a standard MIPI camera connector and the signal requirements and pin count are a very good match to mDP. Plus cabling is easily available. See Section 3.7 more much more about MIPI connections.

Table 3-17 MIPI CSI-2 Camera Connector

Agate Breakout Cable mDP Connector Pin	Wire Type	Signal Name
1	TP+S Pair 1	GND
3	TP+S Pair 1	MIPI_D0P
5	TP+S Pair 1	MIPI_D0N
7	TP+S Pair 2	GND
9	TP+S Pair 2	MIPI_D1P
11	TP+S Pair 2	MIPI_D1N
13	TP+S Pair 3	GND
15	TP+S Pair 3	MIPI_D2P
17	TP+S Pair 3	MIPI_D2N
8	TP+S Pair 4	GND
10	TP+S Pair 4	MIPI_D3P
12	TP+S Pair 4	MIPI_D3N
14	TP+S Pair 5	GND
16	TP+S Pair 5	MIPI_CKN
18	TP+S Pair 5	MIPI_CKP
4	Straight	XMIP_SCL
6	Straight	XMIP_SDA
20	Straight	FP_PWR (3.3V)
19	Straight	GNDp

Note: Shaded sets are shielded twisted pairs with ground

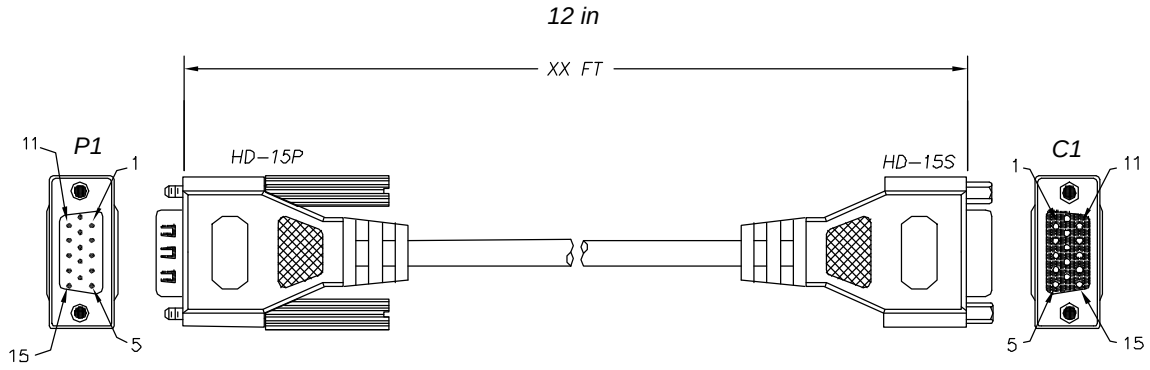
3.12 VGA to VGA Cable

Because two VGA connectors are a tight fit on a PMC board, some VGA connector moldings are too wide to allow two cables to be plugged in simultaneously. Rastergraf can supply cables that are known to fit.

Table 3-18 VGA to VGA Cable (A31-00599-1012)

VGA (P1) Pin	VGA (C2) Pin	Wire Type	Description	
			Function	Name
2	2	75 coax #G	VGA	Green
7	7	75 coax #G	VGA	Green Ground
3	3	75 coax #B	VGA	Blue
8	8	75 coax #B	VGA	Blue Ground
1	1	75 coax #R	VGA	Red
6	6	75 coax #R	VGA	Red Ground
14	14	TP+S #V	VGA	VS
10	10	TP+S #V	VGA	Sync Ground
13	13	TP+S #H	VGA	HS
11	11	TP+S #H	VGA	Ground
12	12	straight	DVI/VGA	SDA
15	15	straight	DVI/VGA	SCL
5	5	straight	DVI/VGA	DDC Ground
9	9	straight	F5V	

Figure 3-20 VGA to VGA Extension Cable (A31-00599-1012)



3.13 LVDS Cable (AgatePXC/1L)

The typical AgatePXC/1L LVDS Cable has two male SDR26 connectors. It is used on the AgatePXC/1L version which has the SDR26 connector documented in Section 3.4.

A typical cable might be a 2 meter SDR to SDR cable. There are several sources for this cable. All of these are 2 meter, but in all cases, other lengths are available:

1) Lynn Products: C20521A-02

2) Pureformance: C20521A-02

3) Intercon 1: MCLCP-2.0-MP

4) 3M 1SF26-L20-00C-200

These cables are standard Mini Camera Link cables, but PoCL versions will also work as the Agate does not use pins 1 and 26.

Other versions of LVDS cables are available:

Pureformance LVDS Cables for use with AgatePXC/1L

Lynn Products LVDS Cables for use with AgatePXC/1L

Referring to the table on the following page, you will see that the connections are mostly NOT wired pin to pin. The Agate wiring follows the "CN-1" end, "Full Configuration" for Mini Camera Link.

Please note that as of this writing none of these cables have been verified.

Figure 3-21 AgatePXC/1L SDR to SDR LVDS Cable

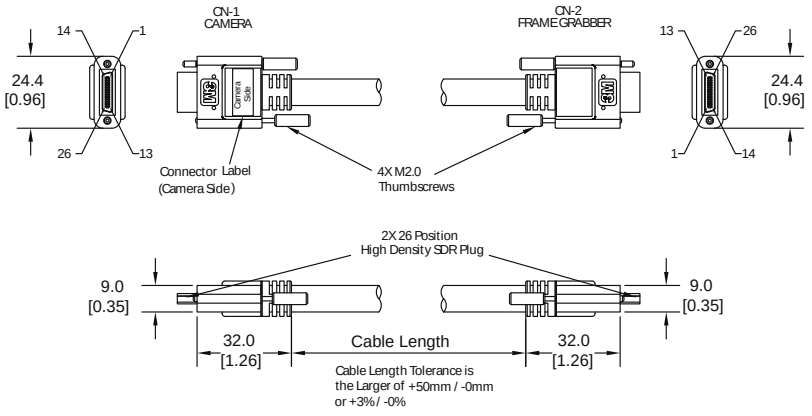


Table 3-19 AgatePXC/1L SDR to SDR LVDS Cable

Agate side SDR26	Far end SDR26	Wire	Description	
Pin	**Pin**	**Type**	**Function**	**Name**
2	25	TWINAX_1_X0-	LVDS Data	R_LVDS_U3P
15	12	TWINAX_1_X0+	LVDS Data	R_LVDS_U3N
3	24	TWINAX_2_X1-	LVDS Data	R_LVDS_U2P
16	11	TWINAX_2_X1+	LVDS Data	R_LVDS_U2N
4	23	TWINAX_3_X2-	LVDS Data	R_LVDS_U1P
17	10	TWINAX_3_X2+	LVDS Data	R_LVDS_U1N
5	22	TWINAX_4_XC-	LVDS Data	R_LVDS_U0P
18	9	TWINAX_4_XC+	LVDS Data	R_LVDS_U0N
6	21	TWINAX_5_X3-	LVDS Data	R_LVDS_UCP
19	8	TWINAX_5_X3+	LVDS Data	R_LVDS_UCN
7	20	TWINAX_6_TC+	LVDS Data	R_LVDS_L3P
20	7	TWINAX_6_TC-	LVDS Data	R_LVDS_L3N
8	19	TWINAX_7_TFG-	LVDS Data	R_LVDS_L2P
21	6	TWINAX_7_TFG+	LVDS Data	R_LVDS_L2N
9	18	TWINAX_8_CC1-	LVDS Data	R_LVDS_L1P
22	5	TWINAX_8_CC1+	LVDS Data	R_LVDS_L1N
10	17	TWINAX_9_CC2-	LVDS Data	R_LVDS_L0P
23	4	TWINAX_9_CC2-	LVDS Data	R_LVDS_L0N
11	16	TWINAX_10_CC3-	LVDS Data	R_LVDS_LCP
24	3	TWINAX_10_CC3+	LVDS Data	R_LVDS_LCN
12	15	TWINAX_11_CC4-	Panel On	R_LVDS_DIGON
25	2	TWINAX_11_CC4+	Panel Vary	R_LVDS_VARY_BL
1	1	Reserved for PoCL	Not used	Not used
14	14	Inner Shield	Ground	Ground
13	13	Inner Shield	Ground	Ground
26	26	Reserved for PoCL	Not used	Not used

3.14 DVI-I Multifunction Breakout Cable (MerlinMTX)

The DVI-I to DVI-D + VGA cable splits out the two functions of the DVI-I connector. This is handy when used with the MerlinMTX PIM (see Section 4.3.3.5).

The cable shown below is the Startech DVI92030202L which is readily available online. The connectors are shown in the same order as is in the table which follows.

Figure 3-22 DVI-I Multifunction Breakout Cable (Startech DVI92030202L)

3.14.1 C1 – VGA

Table 3-20 C1 - VGA Connector

DVI-I Pin	VGA Pin	Wire Type	Description	
			Function	Name
26 (C2)	2	75 coax #G	VGA	Green
30 (C5)	7	75 coax #G	VGA	Green Ground
27 (C3)	3	75 coax #B	VGA	Blue
29 (C5)	8	75 coax #B	VGA	Blue Ground
25 (C1)	1	75 coax #R	VGA	Red
29 (C5)	6	75 coax #R	VGA	Red Ground
8	14	TP+S #V	VGA	VS
22	10	TP+S #V	VGA	Sync Ground
28 (C4)	13	TP+S #H	VGA	HS
11	11	TP+S #H	VGA	Ground
7	12	straight	DVI/VGA	SDA
6	15	straight	DVI/VGA	SCL
11	5	straight	DVI/VGA	DDC Ground
14	9	straight	F5V	

3.14.3 C2 – DVI

Table 3-21 C2 - DVI-D Connector

DVI-I Pin	DVI-D Pin	Wire Type	Description	
			Function	Name
15	15	straight	DVI/VGA	Sync/DDC Ground
7	7	straight	DVI/VGA	SDA
6	6	straight	DVI/VGA	SCL
14	14	straight	F5V	
23	23	TP+S #C	DVI	DVIC_TXCLKP
24	24	TP+S #C	DVI	DVIC_TXCLKN
22	22	TP+S #C	DVI	Pair DCK Ground
18	18	TP+S #0	DVI	DVIC_TX0P
17	17	TP+S #0	DVI	DVIC_TX0N
19	19	TP+S #0	DVI	Pair D0 Ground
10	10	TP+S #1	DVI	DVIC_TX1P
9	9	TP+S #1	DVI	DVIC_TX1N
11	11	TP+S #1	DVI	Pair D1 Ground
2	2	TP+S #2	DVI	DVIC_TX2P
1	1	TP+S #2	DVI	DVIC_TX2N
3	3	TP+S #2	DVI	Pair D2 Ground

3.15 Third-Party Mini DisplayPort Adapters

A variety of dongles that convert DisplayPort to other standard interfaces are available for the Agate and Merlin. Below is a sampling.

Mini DisplayPort (mDP) to VGA Active Adapter (Dongle)

1 x mDP plug to VGA output (receptacle), 1920 x 1200:
StarTech MDP2VGA
available at Amazon

Mini DisplayPort (mDP) to DVI Single Link Active Adapter (Dongle)

1 x mDP plug to DVI-D output (receptacle), 1920 x 1200:
Startech MDP2DVIS
available at Amazon

Mini DisplayPort (mDP) to NTSC/PAL Active Adapter (Dongle)

1 ea mDP plug and USB (for power) to
1 ea RCA (composite) and DIN (S-Video)
1024x768 maximum display resolution output
ViewHD VHDMDP2AV
available at Amazon

3-in-1 Mini DisplayPort to VGA DVI or HDMI converter (Dongle)

1 x mDP plug to:

a) VGA output (receptacle), 1920 x 1200;
b) DVI-D output (receptacle), 1920 x 1200;
c) HDMI output (receptacle), 1920 x 1200

StarTech MDP2VGDVHD
available at Amazon

Mini DisplayPort (mDP) to LVDS Active Adapter (PCB)

VersaLogic Corporation VL-EPH-V6SA
available at Digikey

3.16 MIPI WandCam Adapter (AgatePXC/MerlinPXC)

One problem with MIPI CSI-2 is that while the data transport is a standard, cameras do not have a uniform register set or connector. Also, the MIPI standards are proprietary and it is seriously expensive to gain access to them. So, unless you do that, you have to "trust" the information that you can find on the web.

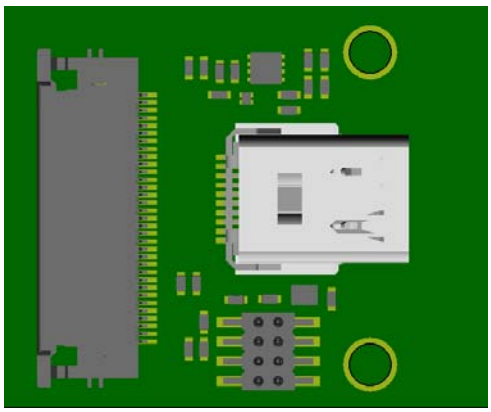
The user manuals for the MIPI cameras by Aptina and OmniVision require NDAs. The manuals don't include software examples, so it is hard to get something running.

The best solution is to use a camera that is supported by whoever makes software you are using. That is why Rastergraf uses the OmniVision OV5640. It is supported by Cypress and e-con systems, Cypress's development partner. The OV5640 is readily available on a little board sold by Avnet as the WandCam.

Rastergraf supports the MIPI camera on both the MerlinPXC and AgatePXC. Included with the AgatePXC or MerlinPXC PIM is a small adapter boardlet that allows you to connect the WandCam to an mDP connector. Then, all you need is an mDP to mDP cable.

We use a Mini DisplayPort (mDP) connector (see Section 3.6) for both the MerlinPXC and the Agate Multifunction Breakout Cable (see Section 3.11) because there isn't a standard MIPI camera connector and the signal requirements and pin count are a very good match to mDP. Plus cabling is readily available.

Figure 3-23 AgatePXC/MerlinPXC MIPI WandCam Paddleboard 3D Model



If you want to use a different camera, it will very likely have a different connector. You can cobble up your own adapter using this handy adapter board or this other one, available from Adafruit. You can also obtain FPC cable as well as FPC connectors. You can use Figure 3-24 (below), the schematic for the AgatePXC WandCam adapter board, as a reference.

You would plug into the Agate breakout cable or the MerlinPXC front panel using a male to female mDP extension cable from CA (Part Number = H713026-01.00). Cut off the female end and tack the cut cable end onto the adapter board. The data pairs are each foil wrapped and include a ground wire. Be sure to connect each of the foil ground wires to a ground pin. MIPI CSI-2 is like DVI in that you MUST HAVE length-matched differential pairs and ALSO all differential pairs must be the same length.

Neither the MerlinPXC connector nor the 50-pin Agate connector include a MIPI Reset pin since not all MIPI cameras use them and those that do generally want just a power-up reset, not a system reset like the Merlin or Agate would supply. So, you should include an RC reset.

Also, MIPI camera may or may not include its own clock. If it doesn't, then you will need to cobble one into your adapter.

Table 3-22 Agate Cable Connections for MIPI WandCam Adapter

Agate Breakout mDP Pin	Signal Name	CA H713026-01.00 Cable Color	Agate WandCam Adapter FPC Pin	Signal Source
1	GND	Bare wire	6	Agate
3	MIPI_D0P	Red	4	Agate
5	MIPI_D0N	White	5	Agate
7	GND	Bare wire	9	Agate
9	MIPI_D1P	Brown	7	Agate
11	MIPI_D1N	White	8	Agate
13	GND	Bare wire	12	Agate
15	MIPI_D2P	Green	10	Agate
17	MIPI_D2N	White	11	Agate
8	GND	Bare wire	15	Agate
10	MIPI_D3P	Blue	13	Agate
12	MIPI_D3N	White	14	Agate
14	GND	Bare wire	3	Agate
16	MIPI_CKN	Black	1	Agate
18	MIPI_CKP	White	2	Agate
n/a	XRST	Gray	31	Adapter
4	XMIP_SCL	White	25	Agate
6	XMIP_SDA	Purple	26	Agate
20	FP_PWR (3.3V)	Pink	27/28	Agate
19	GNDp	Red	24	Agate
n/a	24MHz Clock		29	Adapter
n/a	PWRDN		31	Adapter

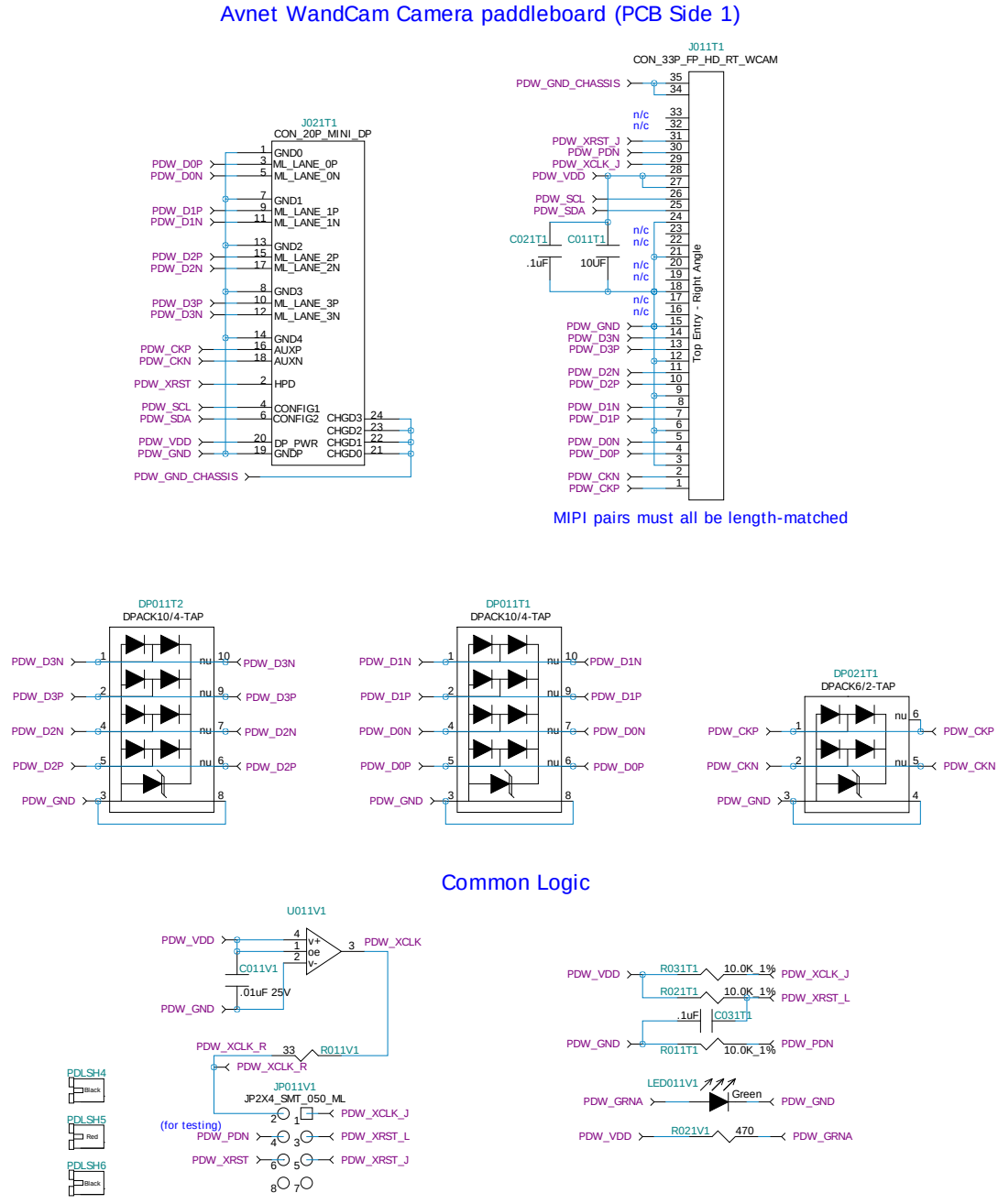
Note: Shaded sets are shielded twisted pairs with ground

Table 3-23 MerlinPXC Front Panel Connector for MIPI WandCam Adapter

MerlinPXC Breakout mDP Pin	Signal Name	CA H713026-01.00 Cable Color	MerlinPXC WandCam Adapter FPC Pin	Signal Source
1	GND	Bare wire	6	MerlinPXC
3	MIPI_D0P	Red	4	MerlinPXC
5	MIPI_D0N	White	5	MerlinPXC
7	GND	Bare wire	9	MerlinPXC
9	MIPI_D1P	Brown	7	MerlinPXC
11	MIPI_D1N	White	8	MerlinPXC
13	GND	Bare wire	12	MerlinPXC
15	MIPI_D2P	Green	10	MerlinPXC
17	MIPI_D2N	White	11	MerlinPXC
8	GND	Bare wire	15	MerlinPXC
10	MIPI_D3P	Blue	13	MerlinPXC
12	MIPI_D3N	White	14	MerlinPXC
14	GND	Bare wire	3	MerlinPXC
16	MIPI_CKN	Black	1	MerlinPXC
18	MIPI_CKP	White	2	MerlinPXC
n/a	XRST	Gray	31	Adapter
4	XMIP_SCL	White	25	MerlinPXC
6	XMIP_SDA	Purple	26	MerlinPXC
20	FP_PWR (3.3V)	Pink	27/28	MerlinPXC
19	GNDp	Red	24	MerlinPXC
n/a	24MHz Clock		29	Adapter
n/a	PWRDN		31	Adapter

Note: Shaded sets are shielded twisted pairs with ground

Figure 3-24 AgatePXC/MerlinPXC MIPI WandCam Paddleboard Schematic



3.17 MerlinPXC PIM VGA Adapter

The MerlinPXC's single channel VGA analog output is available on PMC Pn4 by setting SW1-1 to the off position (see Section 5.6.1).

The MerlinPIM can be supplied with a special-order VGA-only front panel or with the standard MerlinPXC/2-style panel. In the latter case, the VGA can is directed via the mDP connector what is labeled on the MerlinPXC/2 as MIPI.

A side effect of this is that it disables 2 of the 3 DP ports: DP Ch C and F are no longer usable. Only DP Ch D remains. But, if you usually use DP and only need the VGA for debugging, this can be a convenient way to get the VGA without needing the special order PIM.

The MerlinPXC PIM VGA Adapter has an mDP connector and a standard VGA connector. Use a short mDP cable to connect the Adapter to the PIM. An LED on the Adapter indicates that the cable is connected and power is present on the Adapter.

Several switches need to be set correctly to enable this mode:

SW1-1 on the MerlinPXC must be set OFF

SW1-2 on the MerlinPXC PIM must be set OFF

Figure 3-25 MerlinPXC PIM VGA Adapter

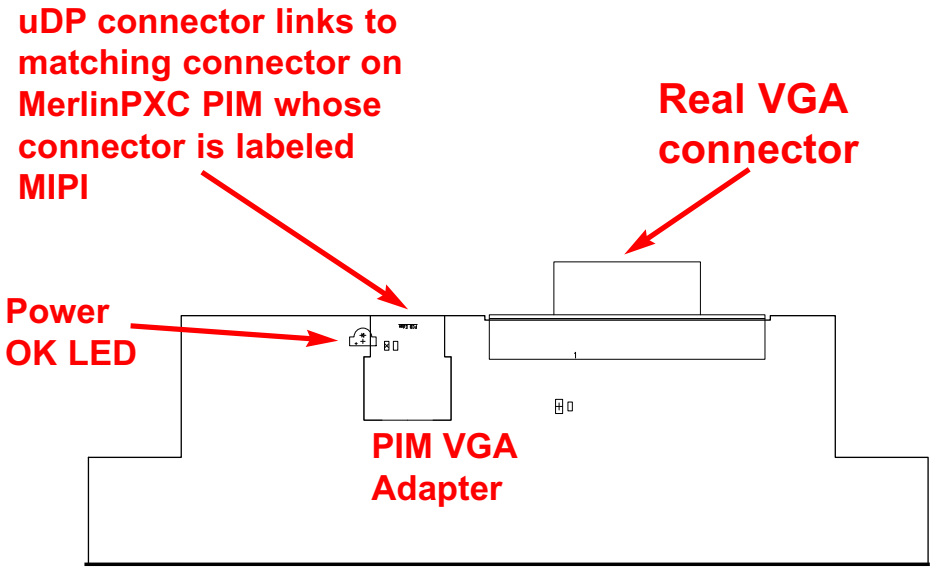


Figure 3-26 MerlinPXC PIM VGA Adapter Schematic

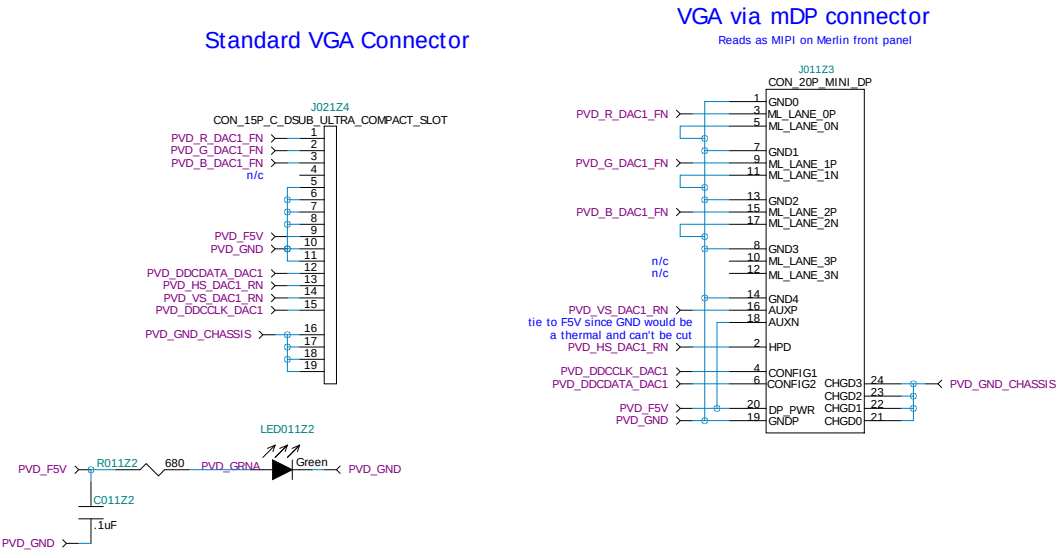
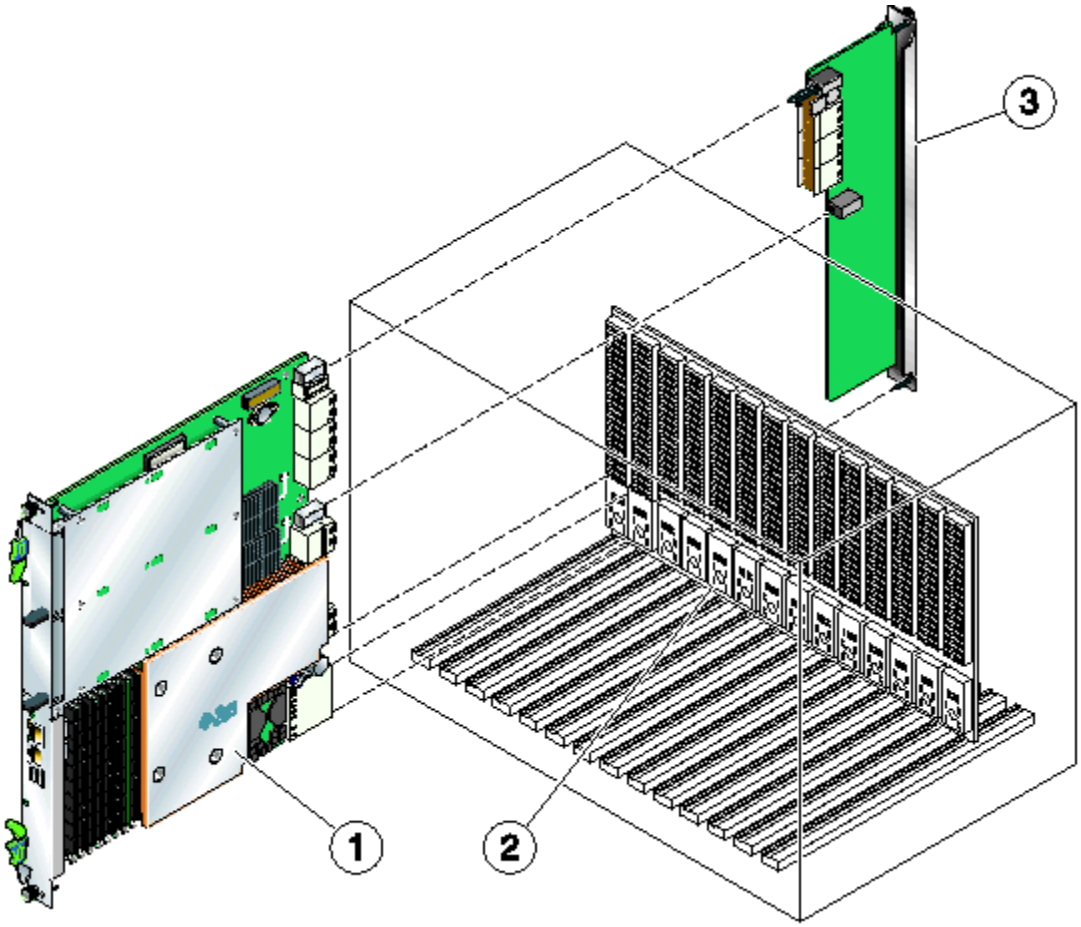


Table 3-24 MerlinPXC PIM VGA Adapter Connections

MerlinPXC PIM mDP "VGA" Pin	MerlinPXC PIM VGA Adapter mDP "VGA" Pin	MerlinPXC PIM VGA Adapter real VGA Pin	Signal Name	Signal Source
1	1	5	PVD_GND	Merlin PIM
3	3	1	PVD_R_DAC1_FN	Merlin PIM
5	5	5	PVD_GND	Merlin PIM
7	7	6	PVD_GND	Merlin PIM
9	9	2	PVD_G_DAC1_FN	Merlin PIM
11	11	6	PVD_GND	Merlin PIM
13	13	7	PVD_GND	Merlin PIM
15	15	3	PVD_B_DAC1_FN	Merlin PIM
17	17	7	PVD_GND	Merlin PIM
8	8	8	PVD_GND	Merlin PIM
14	14	10	PVD_GND	Merlin PIM
16	16	14	PVD_VS_DAC1_RN	Merlin PIM
2	2	13	PVD_HS_DAC1_RN	Merlin PIM
18, 20	18, 20	9	PVD_F5V	Merlin PIM
4	4	15	PVD_DDCCLK_DAC1	Merlin PIM
6	6	12	PVD_DDCDAT_DAC1	Merlin PIM
19	19	11	PVD_GND	Merlin PIM
21, 22, 23, 24	21, 22, 23, 24	16, 17, 18, 19	PVD_GND_CHASSIS	Merlin PIM

Note: Shaded sets are shielded twisted pairs with ground

Chapter 4
Rear I/O Connections



4.1 Introduction

The rear connector sections of the boards are covered in this chapter because there is a lot of material to cover and it makes for a cleaner presentation than mixing in the front panel connectors and cables.

The chapter is organized as follows:

As you will see from the following diagrams, both the AgatePXC and MerlinPXC use PMC Pn4 and XMC Pn6 I/O connectors while the MerlinMTX uses only the PMC Pn4. And you will see that the use of each connector is not duplicated. Some functions are available only on one connector or the other.

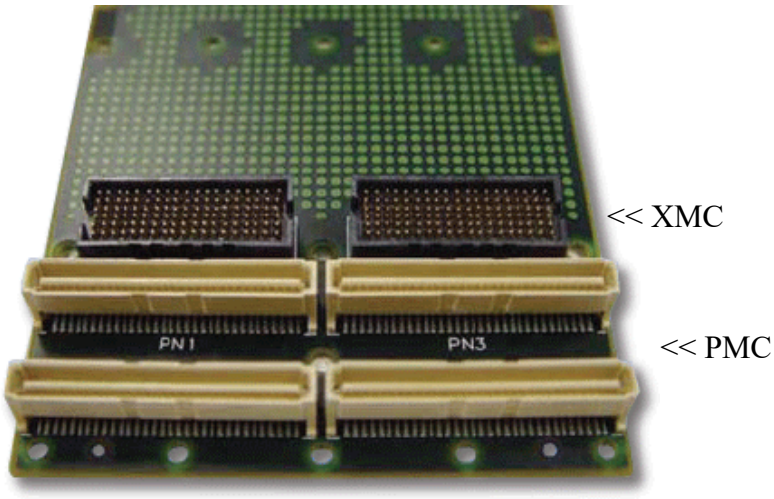
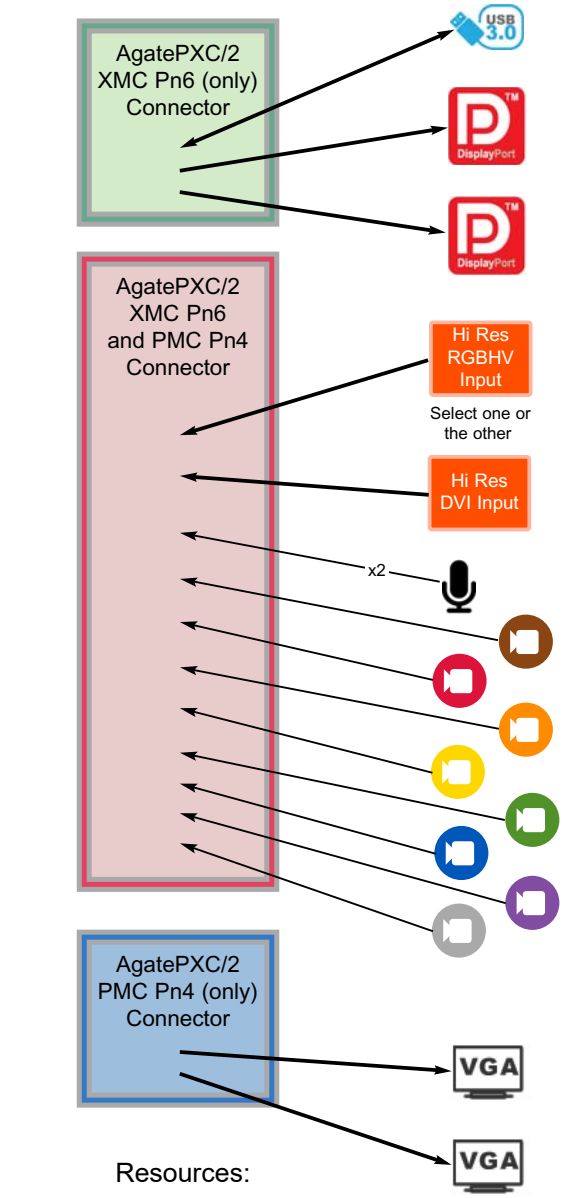


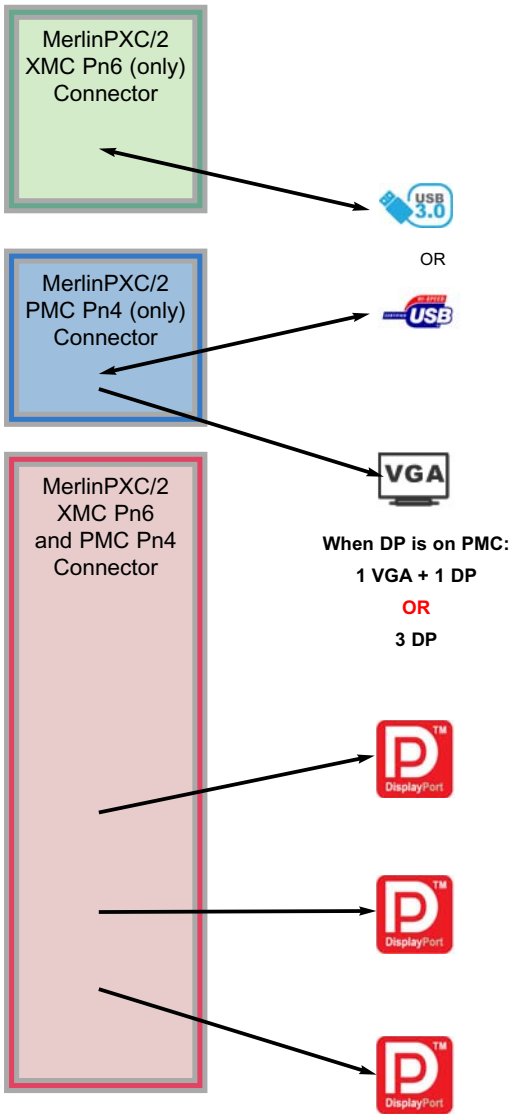
Figure 4-1 AgatePXC/2 Standard Pinout Rear I/O Connections



Resources:

8 NTSC/PAL Video Inputs
2 Audio Inputs
RGBHV or DVI Input
2 DisplayPort **or** 2 VGA
1 USB 3.0

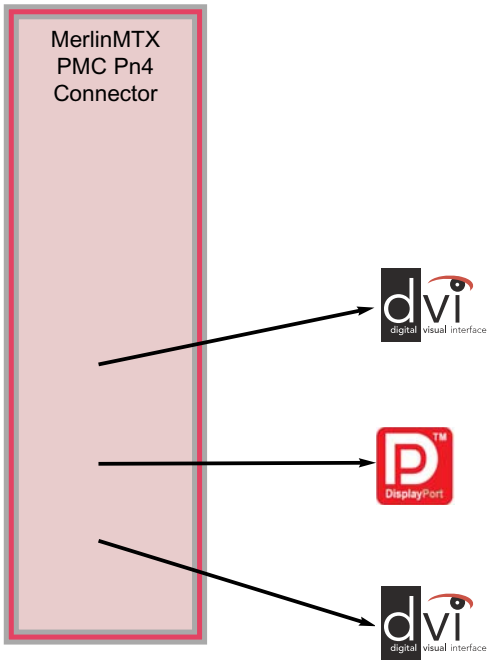
Figure 4-2 MerlinPXC/2 Standard Pinout Rear I/O Connections



Resources:

3 DisplayPort
1 VGA
1 USB 3.0 or 2.0

Figure 4-3 MerlinMTX Standard Pinout Rear I/O Connections



Resources:

2 DVI
1 DisplayPort

4.2 Rear Transition Modules (PIM Carriers)

The Rear Transition Module is a half-length board that plugs into rear of the host system backplane. Thus, connections between the host board (usually a CPU) and the RTM are made as directly as possible. Figure 4-4, provided by Dynamic Engineering, illustrates the concept. The standard 6U RTM is 233.35 x 80mm. The underlying mechanical standards IEEE 1101.10 and 1101.11. The electrical standards are VITA 36 for VME and cPCI and VITA 46.10 for VPX. VITA 36 never actually advanced to a final standard but is used anyway. The standard 6U RTM is 233.35mm x 80 mm and the 3U is 100mm x 80mm. The concept is the same no matter XMC or PMC, VME, cPCI, or VPX.

The PMC I/O Module (PIM) is intended to provide a straightforward way to gain access to the Pn4 and/or Pn6 I/O connectors on a PMC or XMC board. Referring to Figure 4-4, observer that the PIM is mounted on an RTM much like a PMC or XMC card mounts to a host CPU or carrier board. And, the PIM connectors are mapped straight across to the PMC or XMC, providing the shortest possible signal path between the PMC or XMC card and connectors mounted on the PIM board. Thus, instead of having to do the labor-intensive job of tacking on wires or cables, or building a special backplane, the PIM, combined with the RTM, enables clean wiring and connector hookups

Now, it should be noted that some RTMs do not have a PIM location, but many do. In light of this, Rastergraf has designed companion PIMs for its Topaz, Agate, and Merlin graphics boards. Please see the following section (Section 4.3) for more information.

Figure 4-4 PIM Carrier Concept

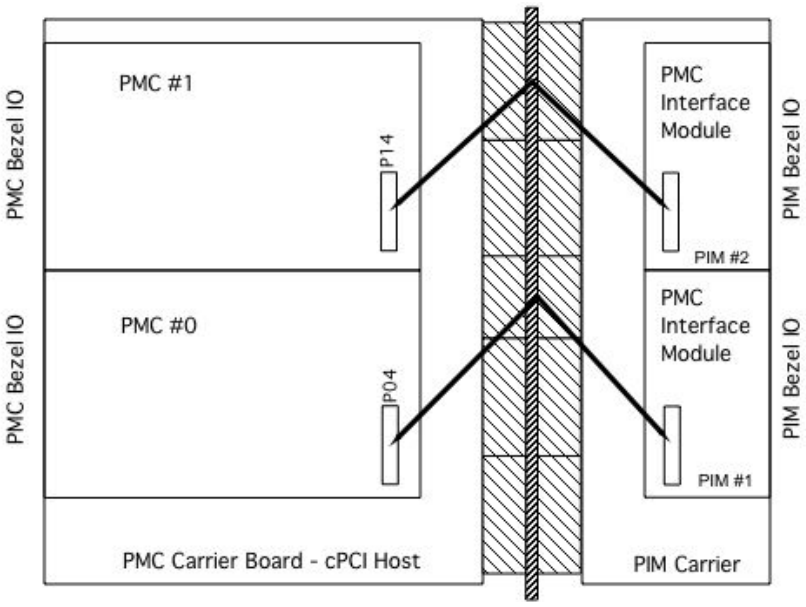


Figure 4-5 Dynamic Engineering PIM-Carrier-Dual

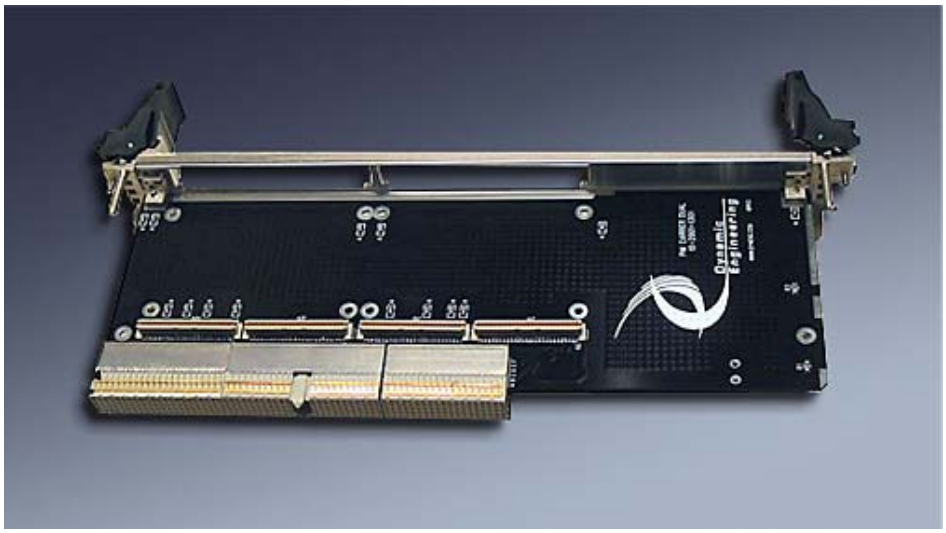


Table 4-1 PIM Carrier Suppliers (not verified or tested)

Vendor	Part Number	Bus	Module Size	Sites	46.9 Support	Usable with Agate or Merlin
Concurrent Technologies	AD PP5/007-03	cPCI J3, J5	6U	2	n/a	Both sites: Agate PMC, Merlin PMC
Dynamic Engineering	PIM-Carrier-Dual	cPCI J3, J5	6U	2	n/a	Both sites: Agate PMC, Merlin PMC
Extreme Engineering	XIt1003	cPCI	6U	2	n/a	Both sites: Agate PMC, Merlin PMC
Sabtech	PC-RTM6U-02	cPCI J3, J4	6U	2	n/a	Both sites: Agate PMC, Merlin PMC
TEWS Technologies	TCP040-TM	cPCI J2	3U	1	n/a	Agate PMC, Merlin PMC
TEWS Technologies	TCP021-TM	cPCI J3, J4	6U	2	n/a	Both sites: Agate PMC, Merlin PMC
ESD	PCIe-XPIMC-Carrier	PCIe	long	1	n/a	Agate PMC, Merlin PMC
Vadatech	PCI100	PCI	long	1	n/a	Agate PMC, Merlin PMC
Extreme Engineering	XIt1010	VME	6U	2	n/a	Both sites: Agate PMC, Merlin PMC
TEWS Technologies	TVME020-TM	VME	6U	2	n/a	Both sites: Agate PMC, Merlin PMC
Extreme Engineering	XIt1044, XIt1041	VPX	6U	2	Both sites: P64s+X12d+X8d	Both sites: Agate PMC, Merlin PMC Both sites: Agate XMC DVI In, USB; Merlin XMC USB
Extreme Engineering	XIt1074	VPX	3U	2	P64s+X12d+X8d	Agate PMC, Merlin PMC Agate XMC DVI In, USB; Merlin XMC USB

4.3 Rastergraf PIMs

4.3.1 AgatePXC PIM

Figure 4-6 AgatePXC PIM Block Diagram

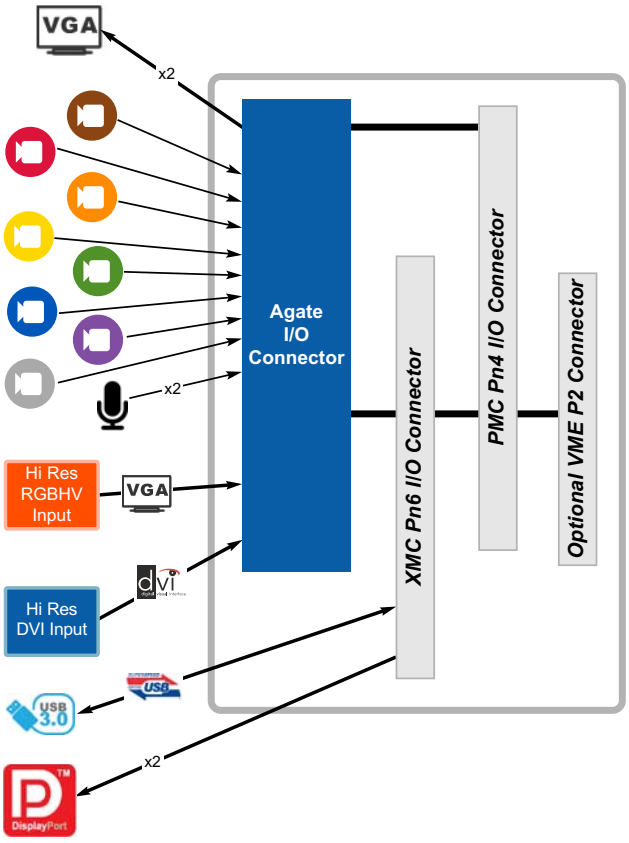
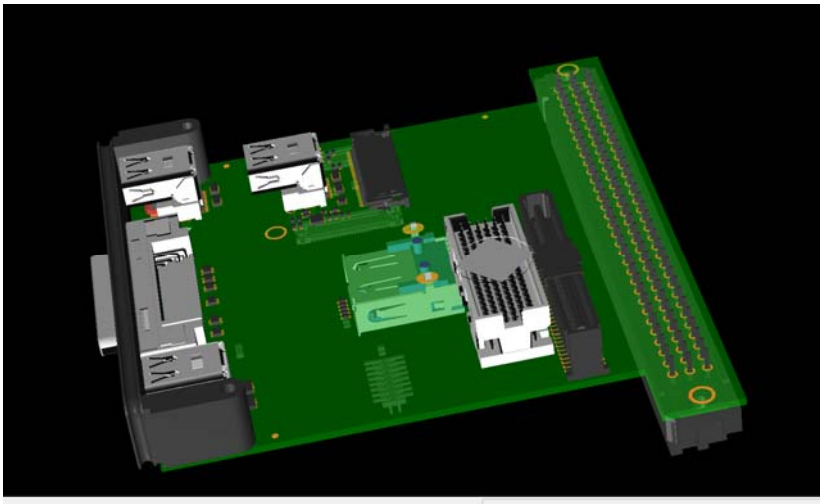


Figure 4-7 AgatePXC PIM 3D Model



4.3.1.1 AgatePXC PIM Introduction

The AgatePXC PIM duplicates the AgatePXC front panel connections, even using the exact same PMC panel. It provides additional connectors for I/O that is not duplicated on the front panel. The standard AgatePXC/2 breakout cable can be used with the PIM.

4.3.1.2 AgatePXC PIM Front Panel Connectors

There are two versions of the AgatePXC PIM available:

a) AgatePXC/1V PIM for AgatePXC/1V and is available by special order only. It includes two VGA connectors.

Please see Section 3.2 for the VGA connectors.

b) AgatePXC/2 PIM for AgatePXC/2. This is the standard PIM. It includes two Mini DisplayPort (mDP) connectors and a Honda SDR50 connector that supplies a multi-mode analog graphics output and audio and video inputs.

Please see Section 3.3 for the Mini DisplayPort connectors.

Please see Section 3.9 for the Honda SDR50 connector.

4.3.1.3 Required Connectivity for the PIM

Note that in order to obtain the full functionality of the Agate PIM, you have to have BOTH PMC Pn4 and XMC Pn6 connected. The following tables detail what PMC and/or XMC connectivity is required for a given function.

We realize that in most cases, you will only have PMC connectivity as only a couple of vendors provide XMC PIM carriers at this time.

Figure 4-8 AgatePXC/1V PIM Front Panel

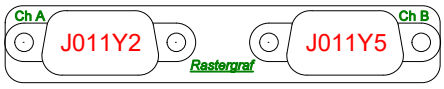


Table 4-2 AgatePXC/1V Required PMC and XMC Connectivity for PIM

On PIM's PMC Pn4 or XMC Pn6?	Signal Set	Required PMC Connectivity	Required XMC Connectivity	PIM Connector	Also on EuroDIN#
PMC only	VGA Ch 1	P64s		J011Y2	yes
PMC only	VGA Ch 2	P64s		J011Y5	yes

 # EuroDIN is VME style connector used with some carriers

Figure 4-9 AgatePXC/2 PIM Front Panel

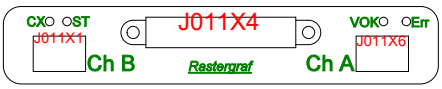


Table 4-3 AgatePXC/2 Required PMC and XMC Connectivity for PIM

On PIM's PMC Pn4 or XMC Pn6?	Signal Set	Required PMC Connectivity		Required XMC Connectivity	PIM Connector	Also on EuroDIN#
both	DVI In	P64s	or	X8d	J011X4	yes
both	VIN1-4	P64s	or	X38s	J011X4	yes
both	RGBHV In*	P64s	or	X24s	J011X4	yes
both	VIN5-8	P64s	or	X24s	J011X4	yes
both	AIN1-2	P64s	or	X24s	J011X4	yes
PMC only	VGA Ch 2	P64s			J011X4	yes
XMC only	DP Ch C			X12d+X38s	J011X6	no
XMC only	DP Ch D			X12d+X24s	J011X1	no
XMC only	USB 3.0			X8d	J012S4	no

* one wire patch required for Agate Rev 2 # EuroDIN is VME style connector used with some carriers

4.3.1.4 AgatePXC PIM EuroDIN Ancillary Connector (J012Q6)

The AgatePXC PIM can be ordered with an additional connector, a EuroDIN 96-pin VME style connector. Both Rastergraf and Technobox supply carriers that are compatible.

You would plug the Agate into the carrier and then plug the PIM into the VME connector on the carrier, thus providing handy access to the PMC Pn4 I/O.

You must specify if the end use is a Rastergraf or Technobox carrier as there is a difference in how the EuroDIN connector is mounted.

4.3.1.5 AgatePXC/2 PIM USB 3.0 Ancillary Connector (J012S4)

If you DO have adequate XMC connectivity, you can make use of the USB 3.0 connector, J012S4, which is located on the back side of the PIM.

4.3.1.5 AgatePXC/2 50-pin Connector (J011X4)

The following table details the pin connections. Note that for DVI In, all pairs must be the same length and the wires in each pair must also be length matched. DP wiring only requires that wires in each pair must be length matched.

Table 4-4 AgatePXC PIM Multi-function I/O Connector Pinout 50C

	SDR Pin	Standard Pinout (50C)	SDR Pin	Standard Pinout (50C)
	1	n/c	26	DVI_IN_1N
	2	DVI_IN_CKN	27	DVI_IN_0N
	3	n/c	28	DVI_IN_1P
	4	DVI_IN_CKP	29	DVI_IN_0P
	5	GND	30	GND
	6	GND	31	GND
	7	DVI_IN_D2N	32	IO_DDCDA_DAC1
Default = HS_C_IN	8	PIM_HS_C_IN_OUT	33	FP_PWR
	9	DVI_IN_D2N	34	IO_DDCCK_DAC1
	10	GND	35	GND
	11	GND	36	PIM_R_IN
	12	PIM_VS_IN_GND_F5	37	PIM _G_IN
	13	FP_VS2	38	PIM _B_IN
	14	PIM _VIN4	39	PIM _VIN8
	15	PIM _VIN2	40	PIM _VIN6
	16	GND	41	GND
	17	GND	42	GND
	18	PIM _VIN3	43	PIM _VIN7
	19	PIM _VIN1	44	PIM _VIN5
	20	PIM_VGA_CH2_RED	45	n/c
Default = DDA	21	PIM_AIN2_CH2_**DDA**	46	PIM_VGA_CH2_HS
	22	GND	47	GND
	23	GND	48	GND
	24	PIM_VGA_CH2_BLU	49	n/c
Default = DDC	25	PIM_AIN1_CH2_**DDC**	50	PIM_VGA_CH2_GRN

4.3.2 MerlinPXC PIM

Figure 4-10 MerlinPXC PIM Block Diagram

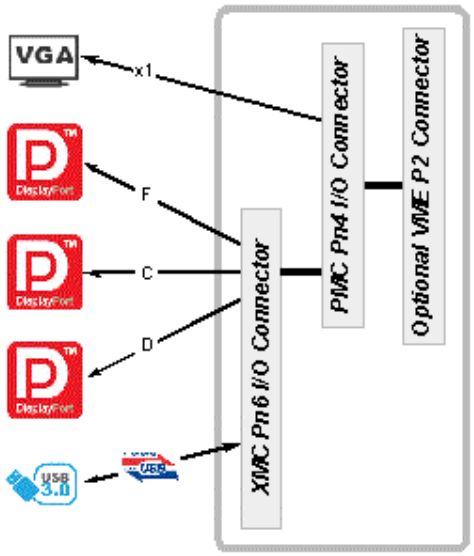
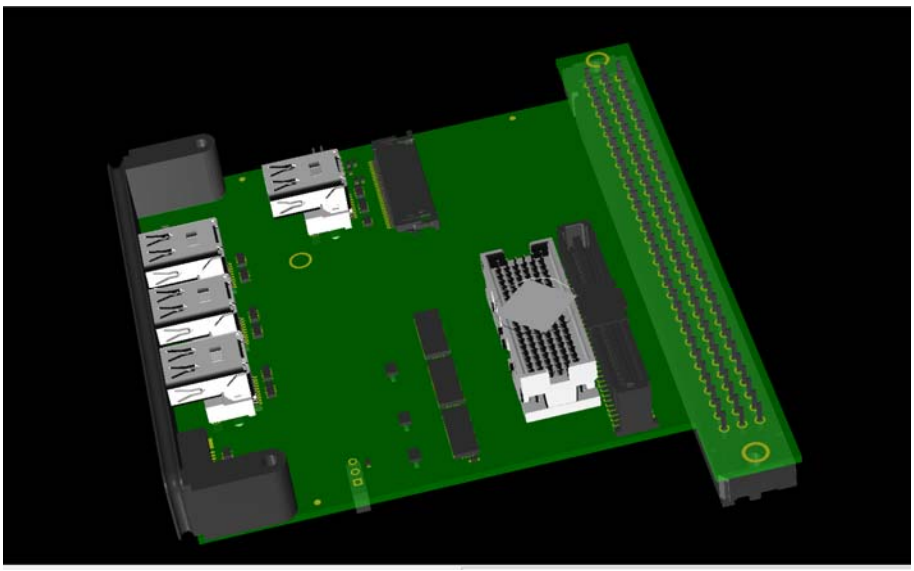


Figure 4-11 MerlinPXC PIM 3D Model



4.3.2.1 MerlinPXC PIM Introduction

The MerlinPXC PIM duplicates the MerlinPXC front panel connections, even using the exact same PMC panel. It provides additional connectors for I/O that is not duplicated on the front panel.

4.3.2.2 MerlinPXC PIM Front Panel Connectors

There are two versions of the MerlinPXC PIM available:

a) MerlinPXC/1V PIM for MerlinPXC/1V and is available by special order only. It includes one VGA connector.

Please see Section 3.2 for the VGA connectors.

b) MerlinPXC/2 PIM for MerlinPXC/2. This is the standard PIM. It includes three Mini DisplayPort (mDP) connectors and a Micro AB USB 3.0 connector.

Please see Section 3.3 for the Mini DisplayPort connectors.

Please see Section 3.5 for the Micro AB USB 3.0 connector.

4.3.2.3 Required Connectivity for the PIM

Note that in order to obtain the full functionality of the MerlinPXC PIM, you have to have BOTH PMC Pn4 and XMC Pn6 connected. The following tables detail what PMC and/or XMC connectivity is required for a given function.

We realize that in most cases, you will only have PMC connectivity as only a couple of vendors provide XMC PIM carriers at this time. In consideration of that, as many connections as possible are duplicated between the XMC and PMC, and in fact, you lose only the USB port if all you have is PMC I/O.

Figure 4-12 MerlinPXC/1V PIM Front Panel

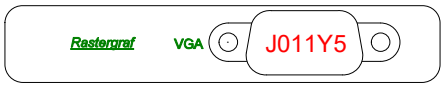


Table 4-5 MerlinPXC/1V Required PMC or XMC Connectivity for PIM

On PIM's PMC Pn4 or XMC Pn6?	Signal Set	Required PMC Connectivity		Required XMC Connectivity	PIM Connector	Also on EuroDIN#
Both	VGA Ch 1	P64s	or	X38s	J011Y5	yes

 # EuroDIN is VME style connector used with some carriers

Figure 4-13 MerlinPXC/2 PIM Front Panel

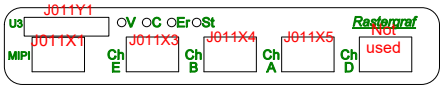


Table 4-6 MerlinPXC/2 Required PMC and XMC Connectivity for PIM

On PIM's PMC Pn4 or XMC Pn6?	Signal Set	Required PMC Connectivity		Required XMC Connectivity	PIM Connector	Also on EuroDIN#
PMC	VGA $	P64s			J011X1	yes
Both*	DP Ch D	P64s	or	X12d+X247s	J011X3	yes
Both*	DP Ch C	P64s	or	X12d+ X8d +X24s	J011X4	yes
Both*	DP Ch F	P64s	or	X12d+X38s	J011X5	yes
XMC only	USB 3.0			X8d	J011Y1	no

$ VGA mode See Section 3.17
* PIM SW1-1 OFF enables DP on PMC and SW1-2 ON enables DP Ch C and F
# EuroDIN is VME style connector used with some carriers

4.3.2.4 MerlinPXC PIM EuroDIN Ancillary Connector (J012Q3)

The MerlinPXC PIM can be ordered with an additional connector, a EuroDIN 96-pin VME style connector. Both Rastergraf and Technobox supply carriers that are compatible.

You would plug the Merlin into the carrier and then plug the PIM into the VME connector on the carrier, thus providing handy access to the PMC Pn4 I/O.

You must specify if the end use is a Rastergraf or Technobox carrier as there is a difference in how the EuroDIN connector is mounted.

4.3.2.5 MerlinPXC/2 PIM USB 3.0 Ancillary Connector (J011Y1)

If you DO have XMC connectivity, you can make use of the USB 3.0 connector, J011Y1, which is located on the front panel of the PIM.

4.3.3 MerlinMTX PIM

Figure 4-14 MerlinMTX PIM Block Diagram

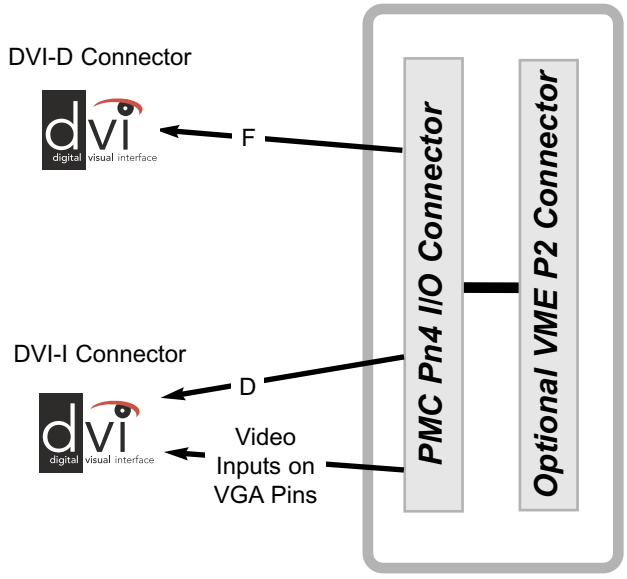
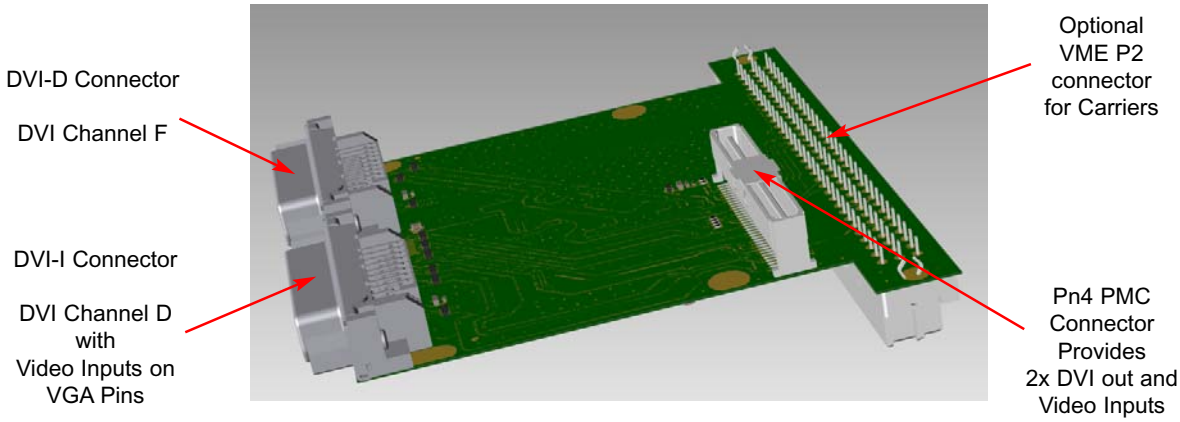


Figure 4-15 MerlinMTX PIM Parts Locations



4.3.3.1 MerlinMTX PIM Introduction

The MerlinMTX PIM provides convenient DVI connectors for the MerlinMTX rear I/O-only DVI ports and audio and video inputs.

4.3.3.2 MerlinMTX PIM Front Panel Connectors

The MerlinMTX PIM includes a DVI-D (DVI only) connector (J011X3) and a DVI-I (DVI+VGA) connector (J011X5). The VGA pins are used for audio and video inputs. See Section 3.8 for information about the use of the DVI-I connector on the MerlinMTX.

4.3.3.3 Required Connectivity for the PIM

Note that in order to obtain the full functionality of the MerlinMTX PIM, you have to have full PMC Pn4. No XMC connectivity is required.

Figure 4-16 MerlinMTX PIM Front Panel

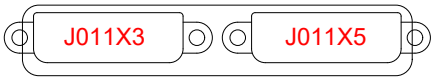


Table 4-7 MerlinMTX Required PMC Connectivity for PIM

Signal Set	Required PMC Connectivity	PIM Connector	Also on EuroDIN#
DP Ch D	P64s	J011X3	yes
DP Ch F	P64s	J011X5	yes

EuroDIN is VME style connector used with some carriers

4.3.3.4 MerlinMTX PIM EuroDIN Ancillary Connector (J012Q3)

The MerlinMTX PIM can be ordered with an additional connector, a EuroDIN 96-pin VME style connector. Both Rastergraf and Technobox supply carriers that are compatible.

You would plug the Agate into the carrier and then plug the PIM into the VME connector on the carrier, thus providing handy access to the PMC Pn4 I/O.

You must specify if the end use is a Rastergraf or Technobox carrier as there is a difference in how the EuroDIN connector is mounted.

4.4 Non-PIM Carriers

While the ideal solution is to use a PIM carrier, there are carriers for PCI and PCIe that accept an PMC or XMC card and use a VME-P2 style connector or wire-wrap pin arrays to break out the connections to the Pn4 or Pn6 I/O connector on the PMC or XMC card.

Both Rastergraf and Technobox make such boards.

Rastergraf has a special version of the AgatePXC PIM and MerlinPXC PIM that allow them to plug directly into the P2 connector. While this can possibly lead to a somewhat unwieldy collection of boards, for prototyping, it is much handier than having to build a special cable.

The following tables list the connections for the Pn4 to P2 style breakout connectors for Agate and Merlin.

Table 4-8 Non-PIM Carrier Suppliers

Vendor	Part Number	Bus	Module Size	Sites	Site Bus	VPWR 5V or 12V	Pn4/Pn6 Breakout	Agate or Merlin PMC or XMC
Rastergraf	PMA-P/P2	PCI	long	1	PMC 32/64	n/a	Pn4 to P2	PMC
Rastergraf	PME-P	PCI	long	1	XMC x4	either	Pn4 to 68 SDR Pn6 to 2x 68 SDR	XMC
Technobox	4933	PCI	long	1	PMC 32/64	n/a	Pn4 to P2	PMC
Technobox	4733	PCIe	long	1	PMC 32/64	n/a	Pn4 to P2	XMC
Technobox	4821	PCIe	long	1	XMC x8	12V	Pn6 to ww pins	XMC
Technobox	5933	PCIe	long	1	XMC x8	either	Pn4	XMC
Technobox	6065	PCIe	long	1	XMC x8	either	Pn4	XMC

.

4.5 PMC and XMC Data Bus Connectors

4.5.1 Connections to PMC Pn1, Pn2, and Pn3

Both the Agate and Merlin PMC connections support the full 64-bit interface as defined in IEEE1368. The 64-bit interface requires Pn1, Pn2, and Pn3. That said, they can all operate at 32-bits (Pn1, Pn2). However, you may not get the desired level of performance.

The PI7C9X130 is capable of supporting 33, 66, 100, and 132 PCI and PCI-X modes, although to be realistic, unless the host CPU or carrier has itself a corresponding PI7C9X130, you are likely to only get 32-bit, 33 MHz out of the typical current chip set PCI bus.

Therefore, if you do intend to use PMC, make sure that you host CPU or carrier DOES have a 9X130 to support the PMC location(s) or you won't get anything like decent performance from the Agate or Merlin. And, some Agate devices won't even try to run.

4.5.2 Connections to XMC Pn5

Both the Agate and Merlin XMC connections support up to an 8-line PCI Express 2.0 (x8 PCIe, 5 Gb/s) serial data bus interface, as defined in VITA 42.0 and VITA 42.3. The boards can also operate at x1 and x4 lane width at PCIe 1.1 (2.5Gb/s) or PCIe 2.0 (5GB/s) maximum data transfer rate.

4.5.3 Performance Expectations

The 33-132MHz PCI and 2.5Gb/s or 5GB/s PCIe transfer speeds really are ideal numbers based on the system clock.

Both PCI and PCIe will be quite slow if you do mostly single byte operations or some other random access operations. Only when doing large block transfers will you approach the maximum rates.

4.5.4 PMC and XMC Data Bus Connection Table

The following pages detail the PMC and XMC data bus connections. Section 4.2 and on cover the rear I/O sections

4.5.5 PMC Pn1 Connector (except MerlinMTX)

Pin	Signal Name	Signal Name	Pin
1	PMC_TCK	n/c	2
3	GND	INTA_L	4
5	INTB_L	INTC_L	6
7	BUSMODE1_L	VCC_PMC	8
9	INTD_L	n/c	10
11	GND	n/c	12
13	PCI_CLK	GND	14
15	GND	GNT_L	16
17	REQ_L	VCC_PMC	18
19	PMC_VIO	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	CBE3_L	26
27	AD22	AD21	28
29	AD19	VCC_PMC	30
31	PMC_VIO	AD17	32
33	FRAME_L	GND	34
35	GND	IRDY_L	36
37	DEVSEL_L	VCC_PMC	38
39	GND	LOCK_L	40
41	n/c	n/c	42
43	PAR	GND	44
45	PMC_VIO	AD15	46
47	AD12	AD11	48
49	AD09	VCC_PMC	50
51	GND	CBE0_L	52
53	AD06	AD05	54
55	AD04	GND	56
57	PMC_VIO	AD03	58
59	AD02	AD01	60
61	AD00	VCC_PMC	62
63	GND	REQ64_L	64

n/c means no connect – user should not connect to the pin

4.5.6 PMC Pn2 Connector (except MerlinMTX)

Pin	Signal Name	Signal Name	Pin
1	n/c	PMC_TRST_L	2
3	PMC_TMS	PMC_TDO	4
5	PMC_TDI	GND	6
7	GND	n/c	8
9	n/c	n/c	10
11	BUSMODE2_L	VDD	12
13	PCI_RST_L	BUSMODE3_L	14
15	VDD	BUSMODE4_L	16
17	n/c	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	VDD	24
25	IDSEL	AD23	26
27	VDD	AD20	28
29	AD18	GND	30
31	AD16	CBE2_L	32
33	GND	n/c	34
35	TRDY_L	PMC_VDD_J2_36	36
37	GND	STOP_L	38
39	PERR_L	GND	40
41	VDD	SERR_L	42
43	CBE1_L	GND	44
45	AD14	AD13	46
47	PCI_M66EN	AD10	48
49	AD08	VDD	50
51	AD07	n/c	52
53	VDD	n/c	54
55	n/c	GND	56
57	n/c	n/c	58
59	GND	n/c	60
61	ACK64_L	VDD	62
63	Ground	n/c	64

n/c means no connect – user should not connect to the pin

4.5.7 PMC Pn3 Connector (except MerlinMTX)

Pin	Signal Name	Signal Name	Pin
1	n/c	GND	2
3	GND	CBE7_L	4
5	CBE6_L	CBE5_L	6
7	CBE4_L	GND	8
9	PMC_VIO	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	PMC_VIO	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	PMC_VIO	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50
51	GND	AD36	52
53	AD35	AD34	54
55	AD33	GND	56
57	PMC_VIO	AD32	58
59	n/c	n/c	60
61	n/c	GND	62
63	GND	n/c	64

n/c means no connect – user should not connect to the pin

4.5.8 XMC Pn5 Connector (all boards)

Position	A	B	C	D	E	F
1	C_PET_XMC_P0	C_PET_XMC_N0	VDD	C_PET_XMC_P1	C_PET_XMC_N1	XMC_VPWR_J5_F1
2	GND	GND	XMC_TRST_L	GND	GND	PERSTN
3	C_PET_XMC_P2	C_PET_XMC_N2	VDD	C_PET_XMC_P3	C_PET_XMC_N3	XMC_VPWR
4	GND	GND	XMC_TCK	GND	GND	n/c
5	PET_XMC_P4	PET_XMC_N4	VDD	PET_XMC_P5	PET_XMC_N5	XMC_VPWR
6	GND	GND	XMC_TMS	GND	GND	n/c
7	PET_XMC_P6	PET_XMC_N6	VDD	PET_XMC_P7	PET_XMC_N7	XMC_VPWR
8	GND	GND	XMC_TDI	GND	GND	n/c
9	n/c	n/c	n/c	n/c	n/c	XMC_VPWR
10	GND	GND	XMC_TDO	GND	GND	XMC_GA 0
11	PER_XMC_P0	PER_XMC_N0	MBISTL	PER_XMC_P1	PER_XMC_N1	XMC_VPWR
12	GND	GND	XMC_GA1	GND	GND	MPRES_L
13	PER_XMC_P2	PER_XMC_N2	n/c	PER_XMC_P3	PER_XMC_N3	XMC_VPWR
14	GND	GND	XMC_GA2	GND	GND	XMC_MSDA
15	PER_XMC_P4	PER_XMC_N4	n/c	PER_XMC_P5	PER_XMC_N5	XMC_VPWR
16	GND	GND	XMC_MVMRO	GND	GND	XMC_MSCL
17	PER_XMC_P6	PER_XMC_N6	n/c	PER_XMC_P7	PER_XMC_N7	n/c
18	GND	GND	n/c	GND	GND	n/c
19	XMC_REF+	XMC_REF-	n/c	n/c	n/c	n/c

Note: n/c means no connect – user should not connect to the pin.
GND = Ground = 0V, XMC_VPWR = 5V or 12V, VDD = 3.3V
Differential Pairs are shaded

The table above follows PCIe Electromechanical Specification (PCIeES) naming conventions. Note that for some reason VITA 42.3 Section 4.2.3 swaps the R and T part of the data pair naming relative to the definition provided in PCIeES (1.1) Section 5.1.

VPWR can be 5V or 12V. See Section 4.5 for more information about power.
GA0, GA1, GA2, MPRES#, and MVMRO not used. Pulled up to 3.3V thru 5.1K
MRSTI# connected to PCI/PCI-X RESET#.
MSDA connected to PCI/PCI-X SDA, MSCL connected to PCI/PCI-X SCL
JTAG signals connected to PCI/PCI-X signals. JTAG I/O looped thru XMC board

4.6 PMC Pn4 and XMC Pn6 I/O Connectors

4.6.1 Introduction

In addition to being able to connect to the Agate or Merlin on the front panel of the board, it is also possible to connect via two of the host/carrier bus connectors at the opposite end of the board. The bus connectors mate with connectors on the host/carrier board, and the signals are then conveyed to the host/carrier backplane connectors.

The principal reason for doing this is that systems used in some applications are completely sealed up and have room to access I/O only via backplane connections.

The main problem with the rear access method is that one does not always have good control over the signal path. Why?

The rear I/O access connector access path consists of the following parts:

a) the internal board connections leading the to Agate or Merlin rear access connectors, PMC Pn4 and XMC Pn6. In some cases the connections are duplicated on both connectors.

b) the mating connectors on the host CPU or carrier board;

c) the PCB wiring from the mating connectors to the backplane connectors on host CPU or carrier board;

d) the backplane connectors themselves

e) the mating connectors on the backplane. In order to connect to these, the backside of the backplane must have pins fed through from the mating connectors. While this may seem obvious, a lot of backplanes don't have those pins.

Now, at this point you can connect directly to the mating connector pins or do it via a PIM/carrier assembly or some other sort of Rear Transition Module (RTM) as it is called.

This rest of this chapter includes information about the various buses that you can plug into, RTMs, PMC Interface Modules (PIMs), P4 and P6 connections, and some wirelists.

4.6.2 Applicable Technical Standards

The Agate and Merlin are designed to work (and indeed DO work) in both PMC and XMC systems using rear XMC Pn6 and/or PMC Pn4 rear I/O connectors.

There are three approved standards that specify ways to route PMC or XMC I/O to the host bus connectors:

a) ANSI/VITA 35-2000:
PMC-P4 Pin Out Mapping To VME-P0 and VME64x-P2

b) ANSI/VITA 46.9-2010:
PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard.

c) PICMG 2.3 R1.0:
PMC on Compact PCI

c) PICMG CPCI-S.0 R2.0:
CompactPCI Serial Basic Specification. Doesn't have any PMC or XMC specific information.

Several bus systems are commonly used with PMC and/or XMC:

1) VME (and its related versions)
2) CompactPCI
3) OpenVPX
4) PCI (common PC systems)
5) PCIe (common PC systems)
6) CompactPCI Serial (and its related versions)

Of these, CompactPCI Serial is the newest and at this point, appears to have no commercially available products that support XMC or PMC rear I/O access.

There are no rear I/O access pins on PCI and PCIe. Side or top connectors are used to map to the Pn4 or Pn6 connectors. Rastergraf makes the PMx series carriers for this purpose.

For the other buses, some PMC or XMC to host bus connector mappings are suitable, but not all. The following pages detail which mappings could work.

Another consideration is the PCB traces on the host CPU or carrier that are used to link the Agate or Merlin to the host bus connector. Only that manufacturer has control over that. Improperly routed, the result will be rear I/O that is unreliable or even unusable. In practice, the traces should be impedance controlled (100 ohms, nom), length-matched differential pairs. The pinouts of both Agate and Merlin depend on this, even for the single-ended lines, which are paired with grounds.

4.7 The Wonderfulness of VITA 46.9

One of the sad things about ANSI/VITA 46.9-2010 is that you can be in compliance with it and still have a solution that will not support the Agate or Merlin. The reason is that VITA 46 permits a partial implementation of the connection scheme. VITA 46.9 is a pile of junk, but it's all we have.

VITA 46.9 has several sub-implementations:

a) P64s - 64 "single-ended" lines on PMC, nevertheless wired as 32 pairs

b) X8d – 8 differential pairs on XMC

c) X12d -12 differential pairs on XMC

d) X38s - 38 "single-ended" lines on XMC, nevertheless wired as 19 pairs

For XMC, VITA 46 allows combinations like:

X8d, X8d+X12d, X8d+X12d+X38s, and so on.

There is also X12d+X8d. It is the same as X8d+X12d but the wiring sets are reversed on the connector – how helpful is that for the typical user?

The following tables show how the XMC sub-standards line align with the Agate and Merlin. **The minimum useful for XMC is X8d+X12d+X24s.**

For PMC, you have to have P64s for everything. Also, take a look at Section 4.3 , which is targeted at PIMs but also contains detailed PMC and XMC connection specifics for each board.

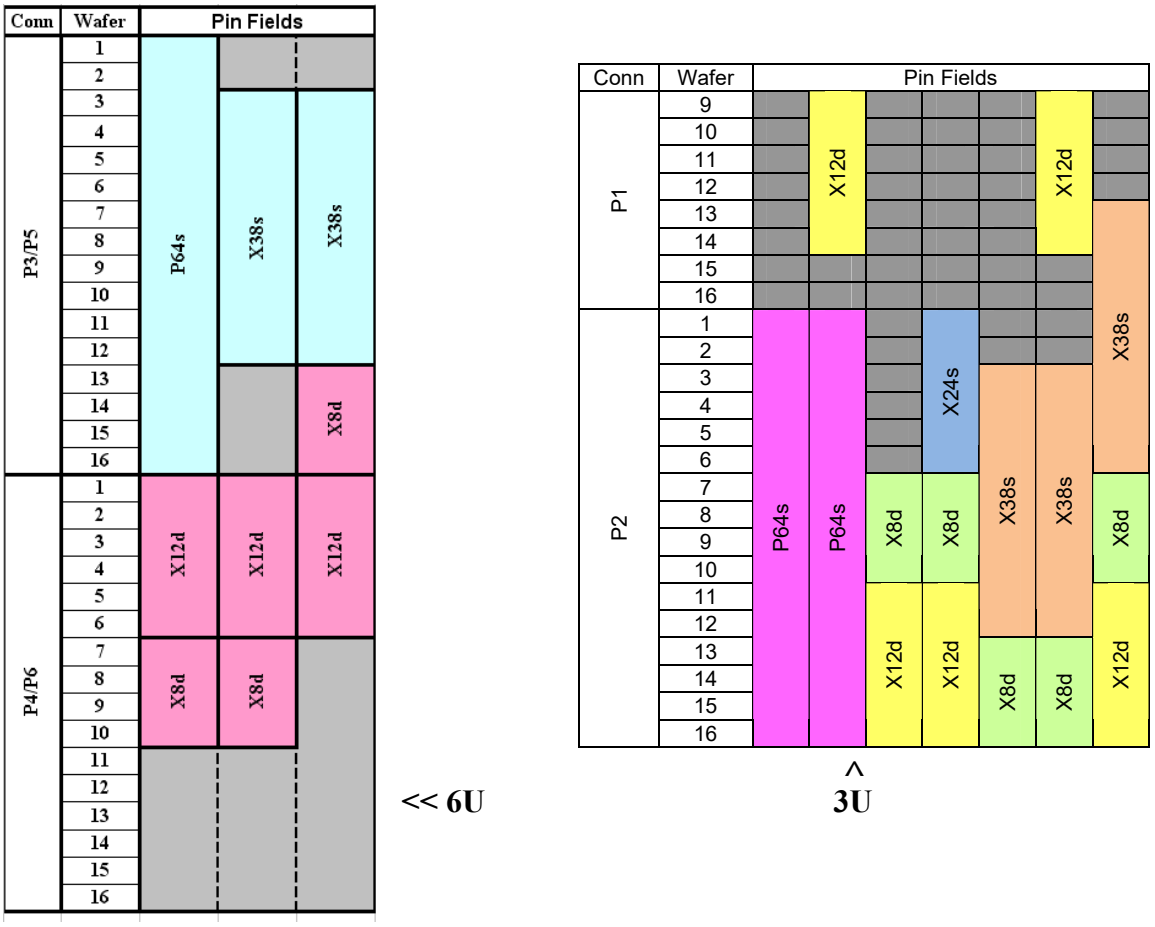
Table 4-9 VITA 46.9 XMC Functionality Requirements

Agate XMC Rear I/O Functionality	Required VITA 46 XMC Function
USB 3.0	X8d
DVI In	X8d
2 Ch DisplayPorts	X12d+X38s
8 Ch NTSC/PAL Input	X38s
2 Ch Audio Input	X38s
RGBHV In	X38s

Merlin XMC Rear I/O Functionality	Required VITA 46 XMC Function
USB 3.0	X8d
3 Ch DisplayPorts	X8d+X12d+X38s
VGA Out	X38s

Note: The MerlinMTX doesn't have any XMC connectors and is therefore omitted.

Table 4-10 VITA 46 6U and 3U VPX Carrier Pin Field Options



In this standard, pin field combinations are named according to how the element pin fields are distributed on the backplane connectors. For example:

P3w1P4-P64s+X12d+X8d defines the composite pin field containing:

1) one P64s pattern map for 64 single-ended contacts on the PMC-Jn4 connector

2) one X12d pattern map for differential pairs on XMC-Jn6 rows 5, 7, 9, 15, 17, and 19

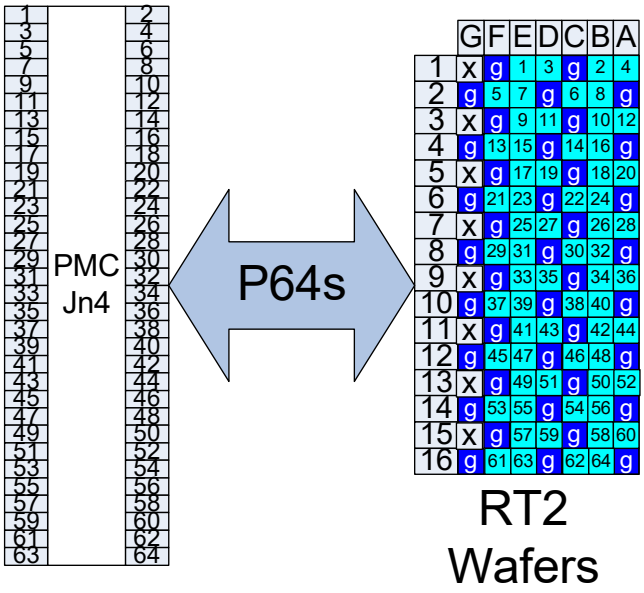
3) one X8d pattern map for differential pairs on XMC-Jn6 rows 1, 3, 11, and 13

with the P64s pin field mapped to the P3 connector starting at wafer 1, the X12d subfield mapped to the P4 connector starting at wafer 1, and the X8d subfield mapped to the P4 connector starting at wafer 7. This is the left-most pin field shown in the left-hand figure above.

The following pages detail the various VITA 46.9, VME, and cPCI Pattern Maps.

Table 4-11 VITA 46.9: PMC to VPX - PMC P64s (AKA P32d)

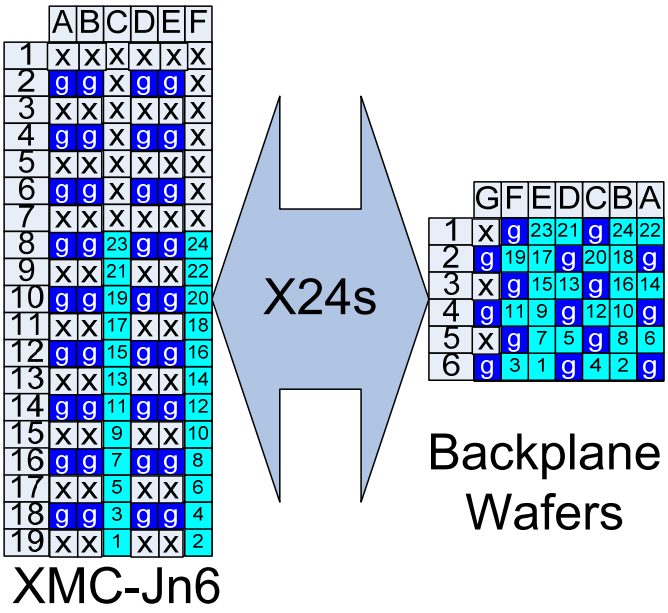
Pattern	Description
P64s	The P64s pattern maps all 64 single-ended contacts on PMC-Jn4 to 16 VPX carrier 7-row RT2 connector differential wafer contacts. It assigns adjacent pins on the same side of the PMC-Jn4 connector forming the pairs on the RT2 connector (Jn4 contacts 1&3; 2&4; etc). The remaining single-ended contacts on the RT2 wafers are not assigned.



Wafer Offset	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		**GND**	Jn4-1	Jn4-3	**GND**	Jn4-2	Jn4-4	P64s
2	**GND**	Jn4-5	Jn4-7	**GND**	Jn4-6	Jn4-8	**GND**	
3		**GND**	Jn4-9	Jn4-11	**GND**	Jn4-10	Jn4-12	
4	**GND**	Jn4-13	Jn4-15	**GND**	Jn4-14	Jn4-16	**GND**	
5		**GND**	Jn4-17	Jn4-19	**GND**	Jn4-18	Jn4-20	
6	**GND**	Jn4-21	Jn4-23	**GND**	Jn4-22	Jn4-24	**GND**	
7		**GND**	Jn4-25	Jn4-27	**GND**	Jn4-26	Jn4-28	
8	**GND**	Jn4-29	Jn4-31	**GND**	Jn4-30	Jn4-32	**GND**	
9		**GND**	Jn4-33	Jn4-35	**GND**	Jn4-34	Jn4-36	
10	**GND**	Jn4-37	Jn4-39	**GND**	Jn4-38	Jn4-40	**GND**	
11		**GND**	Jn4-41	Jn4-43	**GND**	Jn4-42	Jn4-44	
12	**GND**	Jn4-45	Jn4-47	**GND**	Jn4-46	Jn4-48	**GND**	
13		**GND**	Jn4-49	Jn4-51	**GND**	Jn4-50	Jn4-52	
14	**GND**	Jn4-53	Jn4-55	**GND**	Jn4-54	Jn4-56	**GND**	
15		**GND**	Jn4-57	Jn4-59	**GND**	Jn4-58	Jn4-60	
16	**GND**	Jn4-61	Jn4-63	**GND**	Jn4-62	Jn4-64	**GND**	

Table 4-12 VITA 46.9: XMC to VPX - X24s

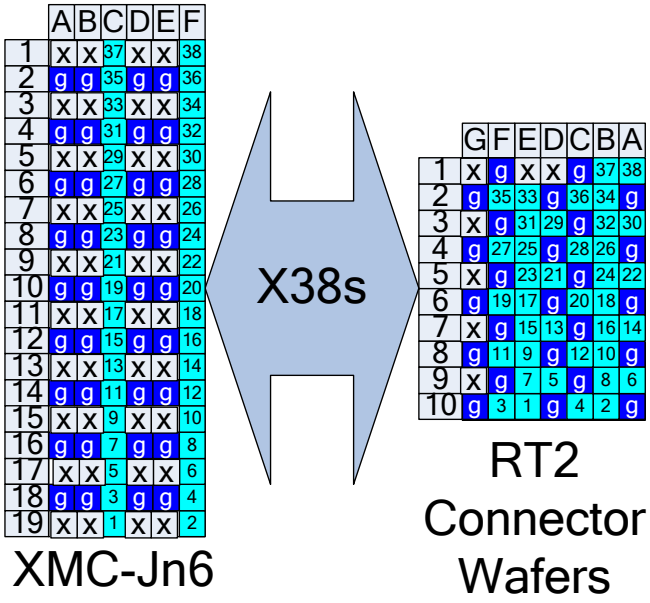
Pattern	Description
X24s	The X24s pattern map provides connections between the 24 single-ended contacts located on rows 8 - 19 on a XMC-Jn6 connector and six VPX carrier 7-row RT2 connector differential pair wafers. Adjacent single-ended contacts on the XMC-Jn6 connector are paired on the differential connector (C8 & C9, F8 & F9, etc). The remaining single-ended contacts on the RT2 wafers are not assigned.



Wafer Offset	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		**GND**	Jn6-C8	Jn6-C9	**GND**	Jn6-F8	Jn6-F9	X24s
2	**GND**	Jn6-C10	Jn6-C11	**GND**	Jn6-F10	Jn6-F11	**GND**	
3		**GND**	Jn6-C12	Jn6-C13	**GND**	Jn6-F12	Jn6-F13	
4	**GND**	Jn6-C14	Jn6-C15	**GND**	Jn6-F14	Jn6-F15	**GND**	
5		**GND**	Jn6-C16	Jn6-C17	**GND**	Jn6-F16	Jn6-F17	
6	**GND**	Jn6-C18	Jn6-C19	**GND**	Jn6-F18	Jn6-F19	**GND**	

Table 4-13 VITA 46.9: XMC to VPX - X38s

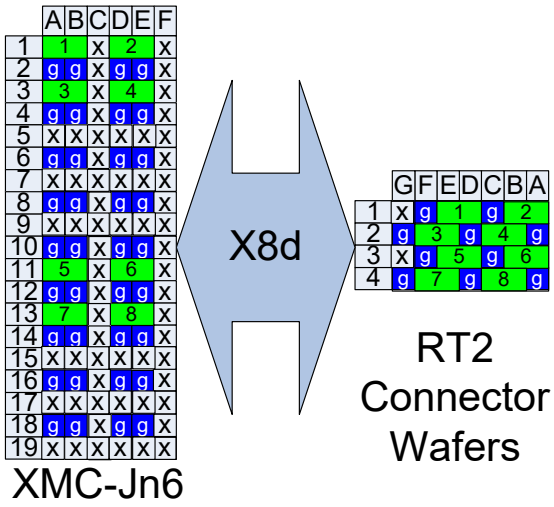
Pattern	Description
X38s	The X38s pattern maps all 38 single-ended contacts on XMC-Jn6 to 10 VPX carrier 7-row RT2 connector differential pair wafers. Adjacent single-ended contacts on the XMC-Jn6 connector are paired on the differential wafers, similar to the pairing used for the PMC-Jn4 contacts on the P64s pattern. The remaining single-ended contacts on the RT2 wafers are not assigned.



Wafer Offset	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		**GND**			**GND**	Jn6-C1	Jn6-F1	X38s
2	**GND**	Jn6-C2	Jn6-C3	**GND**	Jn6-F2	Jn6-F3	**GND**	
3		**GND**	Jn6-C4	Jn6-C5	**GND**	Jn6-F4	Jn6-F5	
4	**GND**	Jn6-C6	Jn6-C7	**GND**	Jn6-F6	Jn6-F7	**GND**	
5		**GND**	Jn6-C8	Jn6-C9	**GND**	Jn6-F8	Jn6-F9	
6	**GND**	Jn6-C10	Jn6-C11	**GND**	Jn6-F10	Jn6-F11	**GND**	
7		**GND**	Jn6-C12	Jn6-C13	**GND**	Jn6-F12	Jn6-F13	
8	**GND**	Jn6-C14	Jn6-C15	**GND**	Jn6-F14	Jn6-F15	**GND**	
9		**GND**	Jn6-C16	Jn6-C17	**GND**	Jn6-F16	Jn6-F17	
10	**GND**	Jn6-C18	Jn6-C19	**GND**	Jn6-F18	Jn6-F19	**GND**	

Table 4-14 VITA 46.9: XMC to VPX - X8d

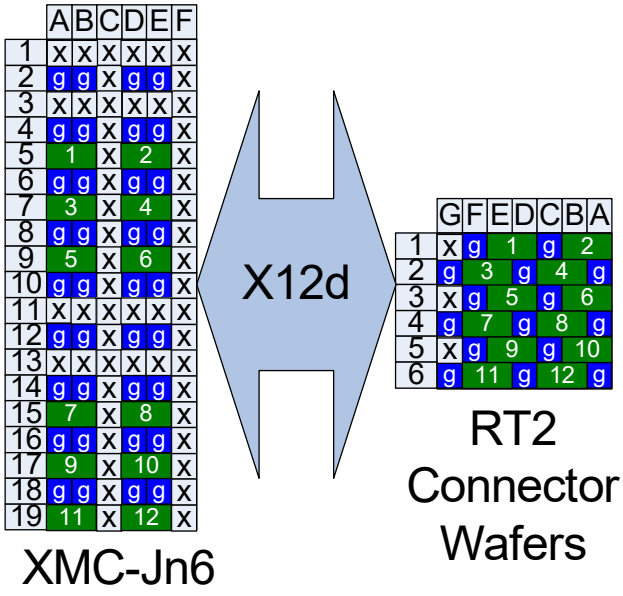
Pattern	Description
X8d	The X8d pattern maps XMC-Jn6 differential pairs on rows 1, 3, 11, and 13 to 4 of the 7-row differential wafers to four VPX carrier 7-row RT2 connector differential pair wafers. The remaining single-ended contacts on the RT2 wafers are not assigned.



Wafer Offset	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		**GND**	Jn6-A1	Jn6-B1	**GND**	Jn6-D1	Jn6-E1	X8d
2	**GND**	Jn6-A3	Jn6-B3	**GND**	Jn6-D3	Jn6-E3	**GND**	
3		**GND**	Jn6-A11	Jn6-B11	**GND**	Jn6-D11	Jn6-E11	
4	**GND**	Jn6-A13	Jn6-B13	**GND**	Jn6-D13	Jn6-E13	**GND**	

Table 4-15 VITA 46.9: XMC to VPX - X12d

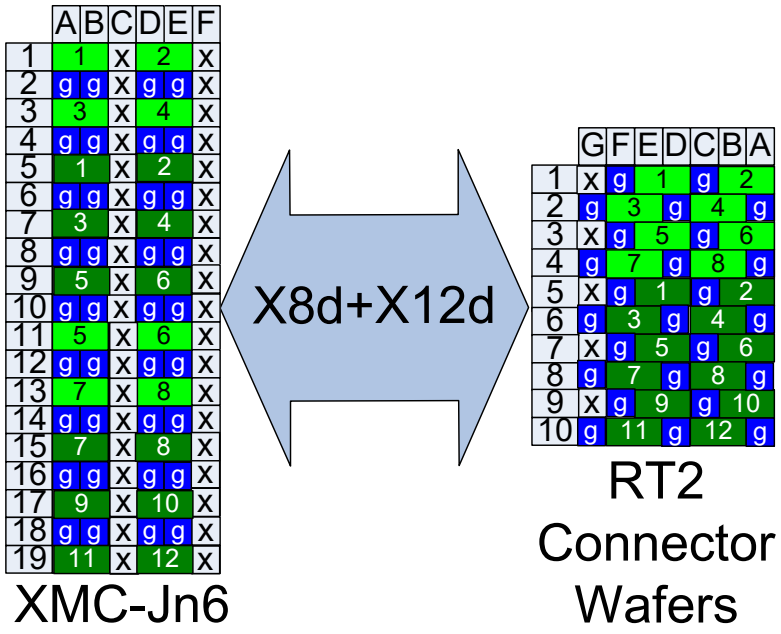
Pattern	Description
X12d	The X12d pattern maps XMC-Jn6 differential pairs on rows 5, 7, 9, 15, 17, and 19 to 6 of the 7-row differential wafers to six VPX 7-row RT2 connector differential pair wafers. The remaining single-ended contacts on the RT2 wafers are not assigned.



Wafer Offset	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		GND	Jn6-A5	Jn6-B5	GND	Jn6-D5	Jn6-E5	X12d
2	GND	Jn6-A7	Jn6-B7	GND	Jn6-D7	Jn6-E7	GND	
3		GND	Jn6-A9	Jn6-B9	GND	Jn6-D9	Jn6-E9	
4	GND	Jn6-A15	Jn6-B15	GND	Jn6-D15	Jn6-E15	GND	
5		GND	Jn6-A17	Jn6-B17	GND	Jn6-D17	Jn6-E17	
6	GND	Jn6-A19	Jn6-B19	GND	Jn6-D19	Jn6-E19	GND	

Table 4-16 VITA 46.9: XMC to VPX - X8d+X12d

Pattern	Description
X8d+X12d	The X8d+X12d pattern maps all 20 differential pairs at the XMC-Jn6 connector to ten VPX 7-row RT2 connector differential pair wafers. This pattern is utilized on both 3U and 6U carriers. The remaining single-ended contacts on the RT2 connector wafers are not assigned.



Wafer Offset	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		GND	Jn6-A1	Jn6-B1	GND	Jn6-D1	Jn6-E1	X8d
2	GND	Jn6-A3	Jn6-B3	GND	Jn6-D3	Jn6-E3	GND	
3		GND	Jn6-A11	Jn6-B11	GND	Jn6-D11	Jn6-E11	
4	GND	Jn6-A13	Jn6-B13	GND	Jn6-D13	Jn6-E13	GND	
5		GND	Jn6-A5	Jn6-B5	GND	Jn6-D5	Jn6-E5	X12d
6	GND	Jn6-A7	Jn6-B7	GND	Jn6-D7	Jn6-E7	GND	
7		GND	Jn6-A9	Jn6-B9	GND	Jn6-D9	Jn6-E9	
8	GND	Jn6-A15	Jn6-B15	GND	Jn6-D15	Jn6-E15	GND	
9		GND	Jn6-A17	Jn6-B17	GND	Jn6-D17	Jn6-E17	
10	GND	Jn6-A19	Jn6-B19	GND	Jn6-D19	Jn6-E19	GND	

4.8 VPX Sample Implementation

It is hard to find a CPUs or carrier that implement a full X8d+X12d+X38S mapping for the XMC connector that the AgatePXC and MerlinPXC boards require for full functionality. PMC is much more common.

Table 4-17 Agate and Merlin VITA 46.9 XMC/PMC Requirements

Board	Functions	VITA 46.9 XMC or PMC
AgatePXC	DisplayPort Ch C	X12d+X38s
	DisplayPort Ch D	X12d+X24s
	USB 3.0	X8d
	DVI In	X8d or P64s
	VIN1-4	X38s or P64s
	RGBHV In*, VIN5-8, AIN1-2	X24s or P64s
	VGA Ch 1, 2	P64s
MerlinPXC	DisplayPort Ch C, D	X12d+X24s or P64s
	DisplayPort Ch F	X12d+X38s or P64s
	VGA	X38s or P64s
	USB 3.0	X8d
MerlinMTX	DVI Ch D, F, DisplayPort Ch C	P64s

Using as examples **CW Defense** and **Acromag** (**GE Automation** does not have this info readily available), we have:

Table 4-18 VITA 46.9 Capabilities of Various CW and Acromag Boards

Vendor	Part Number	Function	Module Size	46.9 Support	Usable with Agate or Merlin
CW Defense	VME-1908/9	CPU	6U	Pn4: P64s	Site P0 and P2: Agate PMC, Merlin PMC
Acromag	ACR5330	Carrier	3U	Pn6: X8d+X12d+X24s	Agate XMC except DP Ch C & VIN1-4 * Merlin XMC DP Ch C, D
CW Defense	VPX6-218	Carrier	6U	Both Sites: Pn4: P64s Pn6: X12d+X8d+X24s	Both sites: Agate PMC, Merlin PMC Agate XMC except DP Ch C & VIN1-4 * Merlin XMC DP Ch C, D
Acromag	ACR5326	Carrier	6U	Pn4: P64s, Pn6: X12d+X8d Pn4: P64s, Pn6: X12d+X8d	Both sites: Agate PMC, Merlin PMC Both sites: Agate XMC DVI In, USB; Merlin XMC USB
CW Defense	VPX3-1259	CPU	3U	X8d+X12d+X24s (full)	Agate XMC except DP Ch C & VIN1-4 * Merlin XMC DP Ch C, D
CW Defense	VPX6-1959	CPU	6U	Pn4: P64s, Pn6: X12d+X8d Pn6: X38s+X12d+X8d	P/XMC Site: Agate PMC, Merlin PMC Site XMC: Agate XMC, Merlin XMC

* Requires one wire patch on Agate Rev 2

4.9 PMC I/O Standard Mappings

The following tables provide the standard mappings for PMC boards for PMC to VME P2 (used on Rastergraf and Technobox PMC carriers) and several mappings of PMC to CompactPCI.

Table 4-19 VITA 35: PMC to VME P2 - Pattern P4V2-64ac

PMC P4	VME P2	PMC P4	VME P2
1	1C	2	1A
3	2C	4	2A
5	3C	6	3A
7	4C	8	4A
9	5C	10	5A
11	6C	12	6A
13	7C	14	7A
15	8C	16	8A
17	9C	18	9A
19	10C	20	10A
21	11C	22	11A
23	12C	24	12A
25	13C	26	13A
27	14C	28	14A
29	15C	30	15A
31	16C	32	16A
33	17C	34	17A
35	18C	36	18A
37	19C	38	19A
39	20C	40	20A
41	21C	42	21A
43	22C	44	22A
45	23C	46	23A
47	24C	48	24A
49	25C	50	25A
51	26C	52	26A
53	27C	54	27A
55	28C	56	28A
57	29C	58	29A
59	30C	60	30A
61	31C	62	31A
63	32C	64	32A

Table 4-20 PICMG 2.3: PMC Slot 1 to cPCI J2

Position	A	B	C	D	E	F
1	S_VI/O	PMC1_IO64	PMC1_IO63	PMC1_IO62	PMC1_IO61	GND
2	PMC1_IO60	PMC1_IO59	PMC1_IO58	PMC1_IO57	PMC1_IO56	GND
3	PMC1_IO55	PMC1_IO54	PMC1_IO53	PMC1_IO52	PMC1_IO51	GND
4	PMC1_IO50	PMC1_IO49	PMC1_IO48	PMC1_IO47	PMC1_IO46	GND
5	PMC1_IO45	PMC1_IO44	PMC1_IO43	PMC1_IO42	PMC1_IO41	GND
6	PMC1_IO40	PMC1_IO39	PMC1_IO38	PMC1_IO37	PMC1_IO36	GND
7	PMC1_IO35	PMC1_IO34	PMC1_IO33	PMC1_IO32	PMC1_IO31	GND
8	PMC1_IO30	PMC1_IO29	PMC1_IO28	PMC1_IO27	PMC1_IO26	GND
9	PMC1_IO25	PMC1_IO24	PMC1_IO23	PMC1_IO22	PMC1_IO21	GND
10	PMC1_IO20	PMC1_IO19	PMC1_IO18	PMC1_IO17	PMC1_IO16	GND
11	PMC1_IO15	PMC1_IO14	PMC1_IO13	PMC1_IO12	PMC1_IO11	GND
12	PMC1_IO10	PMC1_IO9	PMC1_IO8	PMC1_IO7	PMC1_IO6	GND
13	PMC1_IO5	PMC1_IO4	PMC1_IO3	PMC1_IO2	PMC1_IO1	GND
14	VDD	VDD	VDD	VDD	VCC	GND
15	n/c	n/c	n/c	n/c	n/c	GND
16	n/c	n/c	n/c	n/c	n/c	GND
17	n/c	n/c	n/c	n/c	n/c	GND
18	n/c	n/c	n/c	n/c	n/c	GND
19	n/c	n/c	n/c	n/c	n/c	GND
20	n/c	n/c	n/c	n/c	n/c	GND
21	n/c	n/c	n/c	n/c	n/c	GND
22	n/c	n/c	n/c	n/c	n/c	GND

Table 4-21 PICMG 2.3: PMC Slot 0 to cPCI J3

Position	A	B	C	D	E	F
1	S_VI/O	PMC0_IO64	PMC0_IO63	PMC0_IO62	PMC0_IO61	GND
2	PMC0_IO60	PMC0_IO59	PMC0_IO58	PMC0_IO57	PMC0_IO56	GND
3	PMC0_IO55	PMC0_IO54	PMC0_IO53	PMC0_IO52	PMC0_IO51	GND
4	PMC0_IO50	PMC0_IO49	PMC0_IO48	PMC0_IO47	PMC0_IO46	GND
5	PMC0_IO45	PMC0_IO44	PMC0_IO43	PMC0_IO42	PMC0_IO41	GND
6	PMC0_IO40	PMC0_IO39	PMC0_IO38	PMC0_IO37	PMC0_IO36	GND
7	PMC0_IO35	PMC0_IO34	PMC0_IO33	PMC0_IO32	PMC0_IO31	GND
8	PMC0_IO30	PMC0_IO29	PMC0_IO28	PMC0_IO27	PMC0_IO26	GND
9	PMC0_IO25	PMC0_IO24	PMC0_IO23	PMC0_IO22	PMC0_IO21	GND
10	PMC0_IO20	PMC0_IO19	PMC0_IO18	PMC0_IO17	PMC0_IO16	GND
11	PMC0_IO15	PMC0_IO14	PMC0_IO13	PMC0_IO12	PMC0_IO11	GND
12	PMC0_IO10	PMC0_IO9	PMC0_IO8	PMC0_IO7	PMC0_IO6	GND
13	PMC0_IO5	PMC0_IO4	PMC0_IO3	PMC0_IO2	PMC0_IO1	GND
14	VDD (3.3V)	VDD (3.3V)	VDD (3.3V)	VCC (5V)	VCC (5V)	GND
15	n/c	n/c	n/c	n/c	n/c	GND
16	n/c	n/c	n/c	n/c	n/c	GND
17	n/c	n/c	n/c	n/c	n/c	GND
18	n/c	n/c	n/c	n/c	n/c	GND
19	n/c	n/c	n/c	n/c	n/c	GND

Table 4-22 PICMG 2.3: PMC Slot 1 to cPCI J5

Position	A	B	C	D	E	F
1	S_VI/O	PMC1_IO64	PMC1_IO63	PMC1_IO62	PMC1_IO61	GND
2	PMC1_IO60	PMC1_IO59	PMC1_IO58	PMC1_IO57	PMC1_IO56	GND
3	PMC1_IO55	PMC1_IO54	PMC1_IO53	PMC1_IO52	PMC1_IO51	GND
4	PMC1_IO50	PMC1_IO49	PMC1_IO48	PMC1_IO47	PMC1_IO46	GND
5	PMC1_IO45	PMC1_IO44	PMC1_IO43	PMC1_IO42	PMC1_IO41	GND
6	PMC1_IO40	PMC1_IO39	PMC1_IO38	PMC1_IO37	PMC1_IO36	GND
7	PMC1_IO35	PMC1_IO34	PMC1_IO33	PMC1_IO32	PMC1_IO31	GND
8	PMC1_IO30	PMC1_IO29	PMC1_IO28	PMC1_IO27	PMC1_IO26	GND
9	PMC1_IO25	PMC1_IO24	PMC1_IO23	PMC1_IO22	PMC1_IO21	GND
10	PMC1_IO20	PMC1_IO19	PMC1_IO18	PMC1_IO17	PMC1_IO16	GND
11	PMC1_IO15	PMC1_IO14	PMC1_IO13	PMC1_IO12	PMC1_IO11	GND
12	PMC1_IO10	PMC1_IO9	PMC1_IO8	PMC1_IO7	PMC1_IO6	GND
13	PMC1_IO5	PMC1_IO4	PMC1_IO3	PMC1_IO2	PMC1_IO1	GND
14	n/c	n/c	n/c	n/c	n/c	GND
15	n/c	n/c	n/c	n/c	n/c	GND
16	n/c	n/c	n/c	n/c	n/c	GND
17	n/c	n/c	n/c	n/c	n/c	GND
18	n/c	n/c	n/c	n/c	n/c	GND
19	n/c	n/c	n/c	n/c	n/c	GND
20	n/c	n/c	n/c	n/c	n/c	GND
21	n/c	n/c	n/c	n/c	n/c	GND
22	n/c	n/c	n/c	n/c	n/c	GND

Table 4-23 PICMG 2.3: PMC Slot 1 to cPCI J5 (alternate version)

Position	A	B	C	D	E	F
1	n/c	n/c	n/c	n/c	n/c	GND
2	n/c	n/c	n/c	n/c	n/c	GND
3	n/c	n/c	n/c	n/c	n/c	GND
4	n/c	n/c	n/c	n/c	n/c	GND
5	n/c	n/c	n/c	n/c	n/c	GND
6	n/c	n/c	n/c	n/c	n/c	GND
7	n/c	n/c	n/c	n/c	n/c	GND
8	n/c	n/c	n/c	n/c	n/c	GND
9	n/c	n/c	n/c	n/c	n/c	GND
10	S_VI/O	PMC1_IO64	PMC1_IO63	PMC1_IO62	PMC1_IO61	GND
11	PMC1_IO60	PMC1_IO59	PMC1_IO58	PMC1_IO57	PMC1_IO56	GND
12	PMC1_IO55	PMC1_IO54	PMC1_IO53	PMC1_IO52	PMC1_IO51	GND
13	PMC1_IO50	PMC1_IO49	PMC1_IO48	PMC1_IO47	PMC1_IO46	GND
14	PMC1_IO45	PMC1_IO44	PMC1_IO43	PMC1_IO42	PMC1_IO41	GND
15	PMC1_IO40	PMC1_IO39	PMC1_IO38	PMC1_IO37	PMC1_IO36	GND
16	PMC1_IO35	PMC1_IO34	PMC1_IO33	PMC1_IO32	PMC1_IO31	GND
17	PMC1_IO30	PMC1_IO29	PMC1_IO28	PMC1_IO27	PMC1_IO26	GND
18	PMC1_IO25	PMC1_IO24	PMC1_IO23	PMC1_IO22	PMC1_IO21	GND
19	PMC1_IO20	PMC1_IO19	PMC1_IO18	PMC1_IO17	PMC1_IO16	GND
20	PMC1_IO15	PMC1_IO14	PMC1_IO13	PMC1_IO12	PMC1_IO11	GND
21	PMC1_IO10	PMC1_IO9	PMC1_IO8	PMC1_IO7	PMC1_IO6	GND
22	PMC1_IO5	PMC1_IO4	PMC1_IO3	PMC1_IO2	PMC1_IO1	GND

4.10 PMC Pn4 and XMC Pn6 on Agate and Merlin

The “/2” versions of the Agate and Merlin have complete implementations of Pn4 (PMC) and Pn6 (XMC) rear I/O access connections. The other versions have partial implementations based on what the feature set of the board is. The tables on the following pages provide the relevant details.

We strongly urge you to consider using the PIM adapters discussed in Section 4.2 that are available for the Agate and Merlin. They greatly simplify the task of connecting to the boards via the rear I/O.

If, on the other hand, you have to do your own wiring to the backplane connectors, please be aware that many of the signal sets from the Agate and Merlin are differential pairs that REQUIRE matched lengths for each pair, and in the case of DVI, all of the pairs must be the same length.

While it was mentioned earlier in the chapter, it is doesn’t hurt to do it again:

While using rear I/O is very attractive for some applications, there can be some serious difficulties in successfully deploying it. Due to the very high frequency differential signals generated by the USB, DVI and DisplayPort signal sets, great care must be taken in ensuring cleanly routed, equal length traces on the host board between the Pn4 connector and the VME or CPCI backplane connector.

Unless the carrier or host board vendor knew they were routing for the graphics board, this kind of signal routing will not have been done.

For best results, Pn4 connections must be inner-layer matched length for DVI and LVDS signals. Other I/Os require inner-layer signal+ground pairs.

Problems with Pn4 I/O are endemic to PMCs, and are not unique either to the boards in this manual in particular or to graphics boards in general. Before committing to Pn4 solution, it is a good idea to contact the carrier or host board vendor so as to obtain the necessary information to make a good decision. Please contact Rastergraf for assistance.

The following table defines the names and uses for the signals on the Pn4 connector.

The PMC Pn4 Breakout Connector pinout is derived from the VITA 46.9 P64s pinout. Since the VME connector is not appropriate for this product, the 64 pins are mapped as 32 differential pairs wired to a Honda HDRA-EC68LFDT-S-SL+ VHDCI (.8mm) connector.

The pair grouping on PMC Pn4 connector are adjacent pins on the same side of the connector (1,3; 2,4). The pairs are length matched both by pair and over the signal set at 28.425 mm +/- .125 mm (via to via).

Connections are routed as 100Ω differential pairs.

When used as differential pairs, 100Ω round cable (discrete twisted pair cable) MUST BE USED. Ribbon (IDC) cable CANNOT be used because routing limitations prevented matching circuit pairs with ribbon cable pairs.

The rear I/O port is available as USB 3.0 on the XMC Pn6 connector and as a USB 2.0 subset (of the same port) on the PMC Pn4 connector.

Sections 3.14 and 3.15 have wirelists suggesting how a USB cable might be wired to a rear I/O connector. In these cases, you could obtain a USB 3.0 extension cable, cut off the male end, and wire that cable to backplane connector.

The USB 3.0 SuperSpeed pairs are highly sensitive to wire dress and length. It is absolutely CRUCIAL that the SuperSpeed shielded twisted-pair wires be as closely length-matched as possible and that the foil grounds are properly connected. You don’t have to match the RX to the TX, just the RX+ to the RX- and TX+ to TX-.

4.11 Agate PMC Pn4 Connector and Wirelists

Table 4-24 PMC Pn4 Rear Panel Signal Definitions for Agate

Schematic Name	Function	
P4_P6_VINx	NTSC/PAL Video In	
P4_P6_AINx	Audio In	
P4_F5_Vx	Fused 5V for VGA ports. Use at least 24ga wire.	
P4_P6_DVI_INx	DVI In. Use 100Ω shielded, twisted pair	
P4_P6_x_IN	RGBHV In. Use 75Ω Coax	
P4_x_DACy_FN	VGA Channels 1 and 2	
P4_DDCx_y	DDC for VGA Channels 1 and 2	
Schematic Name	**RG-101 Mode (/1R)**	**Standard Mode**
P4_DA_H2	P4_HSYNC_DAC2_RN (HSYNC)	P4_DDCDA_DAC2
P4_P6_VSIN_GND_F5	P4_F5V (PIM) or GND (cable)	P4_P6_VS_IN
P4_GND_G2	P4_G_Y_DAC2_FN (Green)	GND
P4_F5_V2	P4_VSYNC_DAC2_RN (VSYNC)	P4_F5V
P4_H_R2	P4_R_C_DAC2_FN (Red)	P4_HSYNC_DAC1_RN
P4_GND_B2	P4_B_V_DAC2_FN (Blue)	GND
VGA Notes		
Red, Green, and Blue must use 75Ω coax. Each shield must be separately tied to ground. HSYNC and VSYNC should also use 75Ω coax. DDCCK and DDCDA should each be twisted pairs with ground.		

Table 4-25 PMC Pn4 Connector (AgatePXC/2 versions)

Pin	Signal Name	Signal Name	Pin
1	GND	GND	2
3	P4_P6_VIN2	P4_P6_VIN1	4
5	GND	GND	6
7	P4_P6_VIN4	P4_P6_VIN3	8
9	GND	GND	10
11	P4_P6_VIN6	P4_P6_VIN5	12
13	GND	GND	14
15	P4_P6_VIN8	P4_P6_VIN7	16
17	GND	GND	18
19	P4_P6_AIN7	P4_P6_HS_C_IN	20
21	P4_P6_AIN8	GND	22
23	GND	P4_P6_B_IN	24
25	P4_P6_DVI_IN_0P	GND	26
27	P4_P6_DVI_IN_0N	P4_P6_G_IN	28
29	P4_P6_DVI_IN_1P	GND	30
31	P4_P6_DVI_IN_1N	P4_P6_R_IN	32
33	P4_P6_DVI_IN_2P	GND	34
35	P4_P6_DVI_IN_2N	P4_DDCDA_DAC1	36
37	P4_P6_DVI_IN_CP	GND	38
39	P4_P6_DVI_IN_CN	P4_DDCCK_DAC1	40
41	GND	GND	42
43	P4_DDCDA_DAC2 *	P4_F5	44
45	P4_P6_VS_IN *	P4_HSYNC_DAC1_RN	46
47	GND	Ground	48
49	P4_R_C_DAC2_FN	P4_VSYNC_DAC1_RN	50
51	P4_G_Y_DAC2_FN	GND	52
53	GND	P4_B_DAC1_FN	54
55	P4_B_V_DAC2_FN	GND	56
57	P4_HSYNC_DAC2_RN	P4_G_DAC1_FN	58
59	GND	GND	60
61	P4_VSYNC_DAC2_RN	P4_R_DAC1_FN	62
63	P4_DDCCK_DAC2	GND	64

Note: * these two pins were swapped on PCB Rev 0 and 1.

Differential Pairs are shaded

Table 4-26 PMC Pn4 Connector (AgatePXC/1 versions except /1R)

Pin	Signal Name	Signal Name	Pin
1	GND	GND	2
3	n/c	n/c	4
5	GND	GND	6
7	n/c	n/c	8
9	GND	GND	10
11	n/c	n/c	12
13	GND	GND	14
15	n/c	n/c	16
17	GND	GND	18
19	n/c	n/c	20
21	n/c	GND	22
23	GND	n/c	24
25	n/c	GND	26
27	n/c	n/c	28
29	n/c	GND	30
31	n/c	n/c	32
33	n/c	GND	34
35	n/c	P4_DDCDA_DAC1	36
37	n/c	GND	38
39	n/c	P4_DDCCK_DAC1	40
41	GND	GND	42
43	P4_DDCDA_DAC2 *	P4_F5	44
45	n/c *	P4_HSYNC_DAC1_RN	46
47	GND	Ground	48
49	P4_R_C_DAC2_FN	P4_VSYNC_DAC1_RN	50
51	P4_G_Y_DAC2_FN	GND	52
53	GND	P4_B_DAC1_FN	54
55	P4_B_V_DAC2_FN	GND	56
57	P4_HSYNC_DAC2_RN	P4_G_DAC1_FN	58
59	GND	GND	60
61	P4_VSYNC_DAC2_RN	P4_R_DAC1_FN	62
63	P4_DDCCK_DAC2	GND	64

Note: * these two pins are swapped on PCB Rev 0 and 1.

n/c user should not connect to the pin.

Table 4-27 PMC Pn4 Connector – RG-101 Compatible (AgatePXC/1R)

Pin	Signal Name	Signal Name	Pin
1	GND	GND	2
3	n/c	n/c	4
5	GND	GND	6
7	n/c	n/c	8
9	GND	GND	10
11	n/c	n/c	12
13	GND	GND	14
15	n/c	n/c	16
17	GND	GND	18
19	n/c	n/c	20
21	n/c	GND	22
23	GND	n/c	24
25	n/c	GND	26
27	n/c	n/c	28
29	n/c	GND	30
31	n/c	n/c	32
33	n/c	GND	34
35	n/c	n/c	36
37	n/c	GND	38
39	n/c	n/c	40
41	GND	GND	42
43	P4_HSYNC_DAC2_RN	P4_VSYNC_DAC2_RN	44
45	P4_P6_GND_F5	P4_R_C_DAC2_FN	46
47	P4_G_Y_DAC2_FN *	P4_B_V_DAC2_FN	48
49	n/c	n/c	50
51	n/c	GND	52
53	GND	n/c	54
55	n/c	GND	56
57	n/c	n/c	58
59	GND	GND	60
61	n/c	n/c	62
63	n/c	GND	64

Note: n/c means user should not connect to the pin.

* pin = 5V if used with a PIM, GND if used with a cable.

4.11.1 Wirelist: Agate /2 PMC Pn4 to BNC Video Input Connectors

Table 4-28 Wirelist: Agate /2 PMC Pn4 to BNC Video Input Connectors

Pn4 Pin	Pn4 Name	BNC Connector Pin	BNC Cable Name	Cable Type
4	P4_P6_VIN1	1	VIN1	75Ω coax
2	GND	2		Ground
3	P4_P6_VIN2	1	VIN2	75Ω coax
5	GND	2		Ground
8	P4_P6_VIN3	1	VIN3	75Ω coax
6	GND	2		Ground
7	P4_P6_VIN4	1	VIN4	75Ω coax
5	GND	2		Ground
12	P4_P6_VIN5	1	VIN5	75Ω coax
10	GND	2		Ground
11	P4_P6_VIN6	1	VIN6	75Ω coax
9	GND	2		Ground
16	P4_P6_VIN7	1	VIN7	75Ω coax
14	GND	2		Ground
15	P4_P6_VIN8	1	VIN8	75Ω coax
13	GND	2		Ground
32	P4_P6_R_IN	1	R_IN	75Ω coax
30	GND	2		Ground
28	P4_P6_G_IN	1	G_IN	75Ω coax
26	GND	2		Ground
24	P4_P6_B_IN	1	B_IN	75Ω coax
22	GND	2		Ground
20	P4_P6_HS_C_IN	1	HS_C_IN	75Ω coax
18	GND	2		Ground
45	P4_P6_VS_IN	1	VS_IN	75Ω coax
47	GND	2		Ground

4.11.2 Wirelist: Agate /2 PMC Pn4 to RCA Audio Input Connectors

Table 4-29 Wirelist: Agate /2 PMC Pn4 to RCA Audio Input Connectors

Pn4 Pin	Pn4 Name	RCA Connector Pin	RCA Cable Name	Cable Type
19	P4_P6_AIN7	1	AIN7	50Ω coax
17	GND +	2		Ground
21	P4_P6_AIN8	1	AIN8	50Ω coax
17	GND +	2		Ground

+ shared ground pin

4.11.3 Wirelist: Agate /2 PMC Pn4 to DVI Input

Table 4-30 Agate PMC /2 Pn4 to DVI Input Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	DVI-D Pin	DVI-D Name	Cable Type
35	P4_P6_DVI_IN_2N	1	DVI_TX2L	100Ω shielded, twisted pair
33	P4_P6_DVI_IN_2P	2	DVI_TX2H	100Ω shielded, twisted pair
41	GND *	3	DVI_TX2 Shield/Ground	Ground
31	P4_P6_DVI_IN_1N	9	DVI_TX1L	100Ω shielded, twisted pair
29	P4_P6_DVI_IN_1P	10	DVI_TX1H	100Ω shielded, twisted pair
23	GND +	11	DVI_TX1 Shield/Ground	Ground
27	P4_P6_DVI_IN_0N	17	DVI_TX0L	100Ω shielded, twisted pair
25	P4_P6_DVI_IN_0P	18	DVI_TX0H	100Ω shielded, twisted pair
23	GND +	19	DVI_TX0 Shield/Ground	Ground
41	GND *	22	DVI_TXC Shield/Ground	100Ω shielded, twisted pair
37	P4_P6_DVI_IN_CP	23	DVI_TXCH	100Ω shielded, twisted pair
39	P4_P6_DVI_IN_CN	24	DVI_TXCL	Ground

Differential Pairs are shaded +, * shared ground pin

4.11.4 Wirelist: Agate PMC Pn4 to VGA Ch 1 and 2 (all but /1R)

Table 4-31 Agate PMC Pn4 to Standard VGA Ch 1 and 2 Wirelist (all but /1R)

Pn4 Pin	Pn4 Name	VGA Pin	VGA Channel 1 Name	Cable Type
62	P4_R_DAC1_FN	1	Red	75Ω Coax, pin 6 Ground
58	P4_G_DAC1_FN	2	Green	75Ω Coax, pin 7 Ground
54	P4_B_DAC1_FN	3	Blue	75Ω Coax, pin 8 Ground
38	GND *	5	DDC Ground	
64	GND *	6	Red Ground	
60	GND *	7, 8	Green/Blue Ground	
44	P4_F5V +, *	9	Fused +5 Volts, .25A max	5V for DDC, 24ga stranded
52	GND	10	Sync Ground	
42	GND	11	Ground	
36	P4_DDCDA_DAC1	12	DDCDA	Twisted Pair, pin 10 Ground
46	P4_HSYNC_DAC1_RN +	13	HSYNC	Twisted Pair, pin 5 Ground
50	P4_VSYNC_DAC1_RN	14	VSYNC	Twisted Pair, pin 5 Ground
40	P4_DDCCK_DAC1	15	DDCCK	Twisted Pair, pin 10 Ground

Pn4 Pin	Pn4 Name	VGA Pin	VGA Channel 2 Name	Cable Type
49	P4_R_C_DAC2_FN	1	Red	75Ω Coax, pin 6 Ground
51	P4_G_Y_DAC2_FN	2	Green	75Ω Coax, pin 7 Ground
55	P4_B_V_DAC2_FN	3	Blue	75Ω Coax, pin 8 Ground
47	GND *	5	DDC Ground	
53	GND *	6, 7, 8	Red/Green/Blue Ground	
44	P4_F5V +, *	9	Fused +5 Volts, .25A max	5V for DDC, 24ga stranded
59	GND *	10	Sync Ground	
64	GND *	11	Ground	
43	P4_DDCDA_DAC2 +	12	DDCDA	Twisted Pair, pin 10 Ground
57	P4_HSYNC_DAC2_RN	13	HSYNC	Twisted Pair, pin 5 Ground
61	P4_VSYNC_DAC2_RN	14	VSYNC	Twisted Pair, pin 5 Ground
63	P4_DDCCK_DAC2	15	DDCCK	Twisted Pair, pin 10 Ground

+ selected by 0Ω soldered-in jumpers * shared pin

4.11.5 Wirelist: Agate /1R PMC Pn4 to RG-101 VGA

Table 4-32 Agate PMC /1R Pn4 to RG-101 VGA Wirelist

Pn4 Pin	Pn4 Name	VGA Pin	VGA Name	Cable Type
46	P4_R_C_DAC2_FN +	1	Red	75Ω Coax, pin 6 Ground
47	P4_G_Y_DAC2_FN +	2	Green	75Ω Coax, pin 7 Ground
48	P4_B_V_DAC2_FN +	3	Blue	75Ω Coax, pin 8 Ground
45	GND +	6, 7, 8, 10, 11	Ground	Ground
43	P4_HSYNC_DAC2_RN +	13	HSYNC	Twisted Pair, pin 5 Ground
44	P4_VSYNC_DAC2_RN +	14	VSYNC	Twisted Pair, pin 5 Ground

+ selected by 0Ω soldered-in jumpers

4.12 Agate XMC Pn6 Connector and Wirelists

Table 4-33 Pn6 Rear Panel Signal Definitions for Agate

Schematic Name	Function
P4_USB_SSx, Dx	USB 2.0 Data, USB 3.0 Data
P4_USB_V	Switched 5V for USB. Use at least 24ga wire.
XMC_DPCxx	DisplayPort Ch C Data. 100Ω shielded, twisted pair
XMC_DPC_AUXx	DisplayPort Ch C AUX. 100Ω shielded, twisted pair
P6_DPC_x	DisplayPort Ch C Control Signals: PWR, PIN13, HPD, CEC
XMC_DPDxx	DisplayPort Ch D AUX. 100Ω shielded, twisted pair
XMC_DPD_AUXx	DisplayPort Ch D AUX. 100Ω shielded, twisted pair
P6_DPD_x	DisplayPort Ch D Control Signals: PWR, PIN13, HPD, CEC
P4_P6_VINx	NTSC/PAL Video In
P4_P6_AINx	Audio In
P6_F5V	Fused 5V. Use at least 24ga wire.
P4_P6_DVI_INx	DVI In. Use 100Ω shielded, twisted pair
P4_P6_x_IN	RGBHV In. Use 75Ω Coax

Table 4-34 XMC Pn6 Connector (AgatePXC/2 version)

Position	A	B	C	D	E	F
1	P4_USB_DP	P4_USB_DN	GND	P4_USB_SSTXP	P4_USB_SSTXN	P4_P6_VIN1
2	GND	GND	DPC_PWR	GND	GND	GND
3	P4_USB_V	P4_USB_V	DPC_CEC	P4_USB_SSRXP	P4_USB_SSRXN	P4_P6_VIN2
4	GND	GND	GND	GND	GND	GND
5	XMC_DPC_AUXP	XMC_DPC_AUXN	DUMMY_NET1	DPC_PIN13	DPC_HPD	P4_P6_VIN3
6	GND	GND	GND	GND	GND	GND
7	XMC_DPC2P	XMC_DPC2N	P4_P6_HS_C_IN	XMC_DPC3P	XMC_DPC3N	P4_P6_VIN4
8	GND	GND	GND	GND	GND	GND
9	XMC_DPC0P	XMC_DPC0N	P4_P6_VS_IN	XMC_DPC1P	XMC_DPC1N	P4_P6_VIN5
10	GND	GND	DPD_PWR	GND	GND	GND
11	P4_P6_DVI_IN_1P	P4_P6_DVI_IN_1N	DPD_CEC	P4_P6_DVI_IN_0P	P4_P6_DVI_IN_0N	P4_P6_VIN6
12	GND	GND	GND	GND	GND	GND
13	P4_P6_DVI_IN_CP	P4_P6_DVI_IN_CN	DUMMY_NET2	P4_P6_DVI_IN_2P	P4_P6_DVI_IN_2N	P4_P6_VIN7
14	GND	GND	GND	GND	GND	GND
15	XMC_DPD_AUXP	XMC_DPD_AUXN	P4_P6_B_IN	DPD_PIN13	DPD_HPD	P4_P6_VIN8
16	GND	GND	GND	GND	GND	GND
17	XMC_DPD2P	XMC_DPD2N	P4_P6_G_IN	XMC_DPD3P	XMC_DPD3P	P4_P6_AVIN1
18	GND	GND	P4_P6_B_IN	GND	GND	GND
19	XMC_DPD0P	XMC_DPD0N	P6_F5V	XMC_DPD1P	XMC_DPD1P	P4_P6_AVIN2

Note: P4_USB_V & P6_F5V = 5V
Differential Pairs are shaded

Table 4-35 XMC Pn6 Connector (AgatePXC/1x version)

Position	A	B	C	D	E	F
1	n/c	n/c	GND	n/c	n/c	n/c
2	GND	GND	DPC_PWR	GND	GND	GND
3	n/c	n/c	DPC_CEC	n/c	n/c	n/c
4	GND	GND	GND	GND	GND	GND
5	XMC_DPC_AUXP	XMC_DPC_AUXN	DUMMY_NET1	DPC_PIN13	DPC_HPD	n/c
6	GND	GND	GND	GND	GND	GND
7	XMC_DPC2P	XMC_DPC2N	n/c	XMC_DPC3P	XMC_DPC3N	n/c
8	GND	GND	GND	GND	GND	GND
9	XMC_DPC0P	XMC_DPC0N	n/c	XMC_DPC1P	XMC_DPC1N	n/c
10	GND	GND	DPD_PWR	GND	GND	GND
11	n/c	n/c	DPD_CEC	n/c	n/c	n/c
12	GND	GND	GND	GND	GND	GND
13	n/c	n/c	DUMMY_NET2	n/c	n/c	n/c
14	GND	GND	GND	GND	GND	GND
15	XMC_DPD_AUXP	XMC_DPD_AUXN	n/c	DPD_PIN13	DPD_HPD	n/c
16	GND	GND	GND	GND	GND	GND
17	XMC_DPD2P	XMC_DPD2N	n/c	XMC_DPD3P	XMC_DPD3P	n/c
18	GND	GND	n/c	GND	GND	GND
19	XMC_DPD0P	XMC_DPD0N	P6_F5V	XMC_DPD1P	XMC_DPD1P	n/c

Note: n/c means no connect – user should not connect to the pin.
P4_USB_V & P6_F5V = 5V
Differential Pairs are shaded

4.12.1 Wirelist: Agate /2 XMC Pn6 to DisplayPort Channel C

Table 4-36 Agate PMC Pn6 to DisplayPort Channel C Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn6 Pin	Pn6 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
E7	XMC_DPC3N	12	MDPx3N	100Ω shielded, twisted pair
D7	XMC_DPC3P	10	MDPx3P	100Ω shielded, twisted pair
D6	GND	8	Ground	Ground
B7	XMC_DPC2N	17	MDPx2N	100Ω shielded, twisted pair
A7	XMC_DPC2P	15	MDPx2P	100Ω shielded, twisted pair
A6	GND	13	Ground	Ground
E9	XMC_DPC1N	11	MDPx1N	100Ω shielded, twisted pair
D9	XMC_DPC1P	9	MDPx1P	100Ω shielded, twisted pair
D8	GND	7	Ground	Ground
B9	XMC_DPC0N	5	MDPx0N	100Ω shielded, twisted pair
A9	XMC_DPC0P	3	MDPx0P	100Ω shielded, twisted pair
A8	GND	1	Ground	Ground
C3	DPC_CEC	6	MDPx_CEC	
E5	DPC_HPD	2	MDPx_HPD	
C2	DPC_PWR	20	MDPx_PWR	Stranded, 24ga min
D5	DPC_PIN13	4	MDPx_PIN13	
D4	GND	19	GND_PWR	Stranded, 24ga min
B5	XMC_DPC_AUXN	18	MDPx_AUXN	100Ω shielded, twisted pair
A5	XMC_DPC_AUXP	16	MDPx_AUXP	100Ω shielded, twisted pair
A4	GND	14	Ground	Ground

4.12.2 Wirelist: Agate /2 XMC Pn6 to DisplayPort Channel D

Table 4-37 Agate XMC Pn6 to DisplayPort Channel D Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn6 Pin	Pn6 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
E17	XMC_DPD3N	12	MDPx3N	100Ω shielded, twisted pair
D17	XMC_DPD3P	10	MDPx3P	100Ω shielded, twisted pair
D16	GND	8	Ground	Ground
B17	XMC_DPD2N	17	MDPx2N	100Ω shielded, twisted pair
A17	XMC_DPD2P	15	MDPx2P	100Ω shielded, twisted pair
A16	GND	13	Ground	Ground
E19	XMC_DPD1N	11	MDPx1N	100Ω shielded, twisted pair
D19	XMC_DPD1P	9	MDPx1P	100Ω shielded, twisted pair
D18	GND	7	Ground	Ground
B19	XMC_DPD0N	5	MDPx0N	100Ω shielded, twisted pair
A19	XMC_DPD0P	3	MDPx0P	100Ω shielded, twisted pair
A18	GND	1	Ground	Ground
C17	DPD_CEC	6	MDPx_CEC	
C19	DPD_HPD	2	MDPx_HPD	
C16	DPD_PWR	20	MDPx_PWR	Stranded, 24ga min
C18	DPD_PIN13	4	MDPx_PIN13	
C15	GND	19	GND_PWR	Stranded, 24ga min
B9	XMC_DPD_AUXN	18	MDPx_AUXN	100Ω shielded, twisted pair
A9	XMC_DPD_AUXP	16	MDPx_AUXP	100Ω shielded, twisted pair
A8	GND	14	Ground	Ground

4.12.3 Wirelist: Agate /2 XMC Pn6 to USB

Table 4-38 Agate XMC Pn6 to USB Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn6 Pin	Pn6 Name	USB Pin	USB Name	Cable Type
A3	P4_USB_V	1	Switched Power (3.3V)	Stranded, 24ga min
B1	XMC_USB_2_DN	2	USB 2.0 Data N	100Ω shielded, twisted pair
A1	XMC_USB_2_DP	3	USB 2.0 DataP	100Ω shielded, twisted pair
A2	GND	5	Power Ground	Power Ground
E1	P4_USB_SSTXN	6	USB 3.0 SS_TXN	100Ω shielded, twisted pair
D1	P4_USB_SSTXP	7	USB 3.0 SS_TXP	100Ω shielded, twisted pair
D2	GND	8	SS_Ground_Drain	SS_Ground_Drain
E3	P4_USB_SSRXN	9	USB 3.0 SS_RXN	100Ω shielded, twisted pair
D3	P4_USB_SSRXP	10	USB 3.0 SS_RXP	100Ω shielded, twisted pair

4.12.4 Wirelist: Agate /2 XMC Pn6 to BNC Video Input Connectors

Table 4-39 Wirelist: Agate XMC Pn6 to BNC Video Input Connectors

Pn6 Pin	Pn6 Name	BNC Connector Pin	BNC Cable Name	Cable Type
F1	P4_P6_VIN1	1	VIN1	75Ω coax
F2	GND	2		Ground
F3	P4_P6_VIN2	1	VIN2	75Ω coax
F4	GND	2		Ground
F5	P4_P6_VIN3	1	VIN3	75Ω coax
F6	GND	2		Ground
F7	P4_P6_VIN4	1	VIN4	75Ω coax
F8	GND	2		Ground
F9	P4_P6_VIN5	1	VIN5	75Ω coax
F10	GND	2		Ground
F11	P4_P6_VIN6	1	VIN6	75Ω coax
F12	GND	2		Ground
F13	P4_P6_VIN7	1	VIN7	75Ω coax
F14	GND	2		Ground
F15	P4_P6_VIN8	1	VIN8	75Ω coax
F16	GND	2		Ground
C18	P4_P6_R_IN	1	R_IN	75Ω coax
C16	GND +	2		Ground
C17	P4_P6_G_IN	1	G_IN	75Ω coax
C16	GND +	2		Ground
C15	P4_P6_B_IN	1	B_IN	75Ω coax
C14	GND	2		Ground
C7	P4_P6_HS_C_IN	1	HS_C_IN	75Ω coax
C6	GND *	2		Ground
C9	P4_P6_VS_IN	1	VS_IN	75Ω coax
C6	GND *	2		Ground

*, + shared ground pins

4.12.5 Wirelist: Agate /2 XMC Pn6 to RCA Audio Input Connectors

Table 4-40 Wirelist: Agate XMC Pn6 to RCA Audio Input Connectors

Pn6 Pin	Pn6 Name	RCA Connector Pin	RCA Cable Name	Cable Type
F17	P4_P6_AIN7	1	AIN7	50Ω coax
F18	GND +	2		Ground
F19	P4_P6_AIN8	1	AIN8	50Ω coax
F18	GND +	2		Ground

+ shared ground pin

4.12.6 Wirelist: Agate /2 XMC Pn6 to DVI Input

Table 4-41 Agate XMC Pn6 to DVI Input Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn6 Pin	Pn6 Name	DVI-D Pin	DVI-D Name	Cable Type
E13	P4_P6_DVI_IN_2N	1	DVI_TX2L	100Ω shielded, twisted pair
D13	P4_P6_DVI_IN_2P	2	DVI_TX2H	100Ω shielded, twisted pair
D14	GND	3	DVI_TX2 Shield/Ground	Ground
B11	P4_P6_DVI_IN_1N	9	DVI_TX1L	100Ω shielded, twisted pair
A11	P4_P6_DVI_IN_1P	10	DVI_TX1H	100Ω shielded, twisted pair
A12	GND +	11	DVI_TX1 Shield/Ground	Ground
E11	P4_P6_DVI_IN_0N	17	DVI_TX0L	100Ω shielded, twisted pair
D11	P4_P6_DVI_IN_0P	18	DVI_TX0H	100Ω shielded, twisted pair
D12	GND	19	DVI_TX0 Shield/Ground	Ground
A12	GND *	22	DVI_TXC Shield/Ground	100Ω shielded, twisted pair
A13	P4_P6_DVI_IN_CP	23	DVI_TXCH	100Ω shielded, twisted pair
B13	P4_P6_DVI_IN_CN	24	DVI_TXCL	Ground

+ shared ground pin

4.13 MerlinPXC PMC Pn4 Connector and Wirelists

Table 4-42 PMC Pn4 Rear Panel Signal Definitions for Merlin /1x, /2

Schematic Name	Function
PMC_USB_Dx	USB 2.0 Data
P4_USB_V	Switched 5V for USB. Use at least 24ga wire.
P4_F5V	Fused 5V for VGA. Use at least 24ga wire.
PMC_DPCxx	DisplayPort Ch C Data. 100Ω shielded, twisted pair
PMC_DPC_AUXx	DisplayPort Ch C AUX. 100Ω shielded, twisted pair
P6_DPC_x	DisplayPort Ch C Control Signals: PWR, PIN13, HPD, CEC
PMC_DPDxx	DisplayPort Ch D Data. 100Ω shielded, twisted pair
PMC_DPD_AUXx	DisplayPort Ch D AUX. 100Ω shielded, twisted pair
P6_DPD_x	DisplayPort Ch D Control Signals: PWR, PIN13, HPD, CEC
PMC_DPFxx	DisplayPort Ch F Data. 100Ω shielded, twisted pair
PMC_DPF_AUXx	DisplayPort Ch F AUX. 100Ω shielded, twisted pair
P6_DPF_x	DisplayPort Ch F Control Signals: PWR, PIN13, HPD, CEC

Schematic Name	VGA Mode (/1R)	DP Mode (/2)	DVI Mode (/3)
P4_GND_B1	B_DAC1_FN_R (Blue)	GND	GND
P4_GND_G1	G_DAC1_FN_R (Green)	GND	GND
P4_FAN_V1	VS_DAC1_RN_R (VSYNC)	PMC_DPF_AUXN *	PMC_F_DDCDAT
P4_FAP_R1	R_DAC1_FN_R (Red)	PMC_DPF_AUXP *	PMC_F_DDCCLK
P4_CAN_H1	HS_DAC1_RN_R (HSYNC)	PMC_DPC_AUXN *	PMC_DPC_AUXN *
P4_CAP_GND	GND	PMC_DPC_AUXP *	PMC_DPC_AUXP *
P6_FC_DDCL	DDCCLK_DAC1 (DDCCK)	P6_DPF_CEC	P4_P6_VIN6
P6_CC_DDDA	DDCDATA_DAC1 (DDCDA)	P6_DPC_CEC	P6_DPC_CEC

VGA Mode Notes	DP Mode Notes
Red, Green, and Blue must use 75Ω coax with each shield tied to ground. HSYNC and VSYNC should also use 75Ω coax. DDCCK and DDCDA should each be twisted pairs with ground.	* 100Ω shielded, twisted pair

Table 4-43 PMC Pn4 Rear Panel Signal Definitions for Merlin /3

Schematic Name	Function
P4_P6_VINx	NTSC/PAL Video In
P4_P6_VINx_AINx	Shared Video/Audio Input. Build option determines VINx or AINx
P4_F5V	Fused 5V for VGA. Use at least 24ga wire.
PMC_DPCxx	DisplayPort Ch C Data. 100Ω shielded, twisted pair
PMC_DPC_AUXx	DisplayPort Ch C AUX. 100Ω shielded, twisted pair
P6_DPC_x	DisplayPort Ch C Control Signals: PWR, PIN13, HPD, CEC
PMC_TXxx_D	DVI Ch D. 100Ω shielded, twisted pair
PMC_D_DDCxxx	DVI Ch D Control. 100Ω shielded, each DDC paired with ground
P6_DPD_x	DVI Ch D Auxiliary Signals: PWR, HPD
PMC_TXxx_F	DVI Ch F. 100Ω shielded, twisted pair
PMC_F_DDCxxx	DVI Ch F Control. 100Ω shielded, each DDC paired with ground
P6_DPF_x	DVI Ch F Auxiliary Signals: PWR, HPD

Schematic Name	VGA Mode (/1R)	DP Mode (/2)	DVI Mode (/3)
P4_GND_B1	B_DAC1_FN_R (Blue)	GND	GND
P4_GND_G1	G_DAC1_FN_R (Green)	GND	GND
P4_FAN_V1	VS_DAC1_RN_R (VSYNC)	PMC_DPF_AUXN *	PMC_F_DDCDAT
P4_FAP_R1	R_DAC1_FN_R (Red)	PMC_DPF_AUXP *	PMC_F_DDCCLK
P4_CAN_H1	HS_DAC1_RN_R (HSYNC)	PMC_DPC_AUXN *	PMC_DPC_AUXN *
P4_CAP_GND	GND	PMC_DPC_AUXP *	PMC_DPC_AUXP *
P6_FC_DDCL	DDCCLK_DAC1 (DDCCK)	P6_DPF_CEC	P4_P6_VIN6
P6_CC_DDDA	DDCDATA_DAC1 (DDCDA)	P6_DPC_CEC	P6_DPC_CEC

VGA Mode Notes	DP Mode Notes
Red, Green, and Blue must use 75Ω coax with each shield tied to ground. HSYNC and VSYNC should also use 75Ω coax. DDCCK and DDCDA should each be twisted pairs with ground.	* 100Ω shielded, twisted pair

Table 4-44 PMC Pn4 Connector (MerlinPXC/2 versions)

Pin	Signal Name	Signal Name	Pin
1	PMC_USB_2_DN	PMC_DPD_AUXN	2
3	PMC_USB_2_DP	PMC_DPD_AUXP	4
5	P4_USB_V	P4_F5V	6
7	P6_DPF_CEC #	P6_DPF_PWR	8
9	P6_DPF_HPD	P6_DPF_PIN13	10
11	GND	GND	12
13	PMC_DPF3N	PMC_DPF2N	14
15	PMC_DPF3P	PMC_DPF2P	16
17	GND	GND	18
19	PMC_DPF1N	PMC_DPF0N	20
21	PMC_DPF1P	PMC_DPF0P	22
23	GND	GND	24
25	P6_DPC_CEC #	P6_DPC_PWR	26
27	P6_DPC_HPD	P6_DPC_PIN13	28
29	GND	GND	30
31	PMC_DPC3N	PMC_DPC2N	32
33	PMC_DPC3P	PMC_DPC2P	34
35	GND	GND	36
37	PMC_DPC1N	PMC_DPC0N	38
39	PMC_DPC1P	PMC_DPC0P	40
41	GND	GND	42
43	PMC_DPC_AUXN #	PMC_DPF_AUXN #	44
45	PMC_DPC_AUXP #	PMC_DPF_AUXP #	46
47	GND #	GND #	48
49	P6_DPD_CEC	P6_DPD_PWR	50
51	P6_DPD_HPD	P6_DPD_PIN13	52
53	GND	GND	54
55	PMC_DPD3N	PMC_DPD2N	56
57	PMC_DPD3P	PMC_DPD2P	58
59	GND	GND	60
61	PMC_DPD1N	PMC_DPD0N	62
63	PMC_DPD1P	PMC_DPD0P	64

Note: # selected by RG_SEL switch set OFF.
Differential Pairs are shaded

Table 4-45 PMC Pn4 Connector – RG-101 Compatible (MerlinPXC/1R)

Pin	Signal Name	Signal Name	Pin
1	n/c	PMC_DPD_AUXN	2
3	n/c	PMC_DPD_AUXP	4
5	n/c	P4_F5V	6
7	DDCCLK_DAC1 #	n/c	8
9	n/c	n/c	10
11	GND	GND	12
13	n/c	n/c	14
15	n/c	n/c	16
17	GND	GND	18
19	n/c	n/c	20
21	n/c	n/c	22
23	GND	GND	24
25	DDCDATA_DAC1 #	n/c	26
27	n/c	n/c	28
29	GND	GND	30
31	n/c	n/c	32
33	n/c	n/c	34
35	GND	GND	36
37	n/c	n/c	38
39	n/c	n/c	40
41	GND	GND	42
43	HS_DAC1_RN_R #	VS_DAC1_RN_R #	44
45	GND #	R_DAC1_FN_R #	46
47	G_DAC1_FN_R #	B_DAC1_FN_R #	48
49	P6_DPD_CEC	P6_DPD_PWR	50
51	P6_DPD_HPD	P6_DPD_PIN13	52
53	GND	GND	54
55	PMC_DPD3N	PMC_DPD2N	56
57	PMC_DPD3P	PMC_DPD2P	58
59	GND	GND	60
61	PMC_DPD1N	PMC_DPD0N	62
63	PMC_DPD1P	PMC_DPD0P	64

Note: n/c means no connect – user should not connect to the pin.
selected by RG_SEL switch set ON.
Differential Pairs are shaded

Table 4-46 PMC Pn4 Connector, DVI Pinout (MerlinPXC/3)

Pin	Signal Name	Signal Name	Pin
1	P6_DPC_PWR	PMC_D_DDCDAT	2
3	P4_P6_VIN8	PMC_D_DDCLK	4
5	GND	P4_F5V	6
7	P4_P6_VIN6	P6_DPF_PWR	8
9	P6_DPF_HPD	P4_P6_VIN5	10
11	GND	GND	12
13	PMC_F_TMDSCN	PMC_F_TMDS0N	14
15	PMC_F_TMDSCP	PMC_F_TMDS0P	16
17	GND	GND	18
19	PMC_F_TMDS1N	PMC_F_TMDS2N	20
21	PMC_F_TMDS1P	PMC_F_TMDS2P	22
23	GND	P4_P6_VIN7	24
25	P6_DPC_CEC #	GND	26
27	P6_DPC_HPD	P6_DPC_PIN13	28
29	GND	GND	30
31	PMC_DPC3N	PMC_DPC2N	32
33	PMC_DPC3P	PMC_DPC2P	34
35	GND	GND	36
37	PMC_DPC1N	PMC_DPC0N	38
39	PMC_DPC1P	PMC_DPC0P	40
41	GND	GND	42
43	PMC_DPC_AUXN #	PMC_F_DDCDAT #	44
45	PMC_DPC_AUXP #	PMC_F_DDCLK #	46
47	GND #	GND #	48
49	P4_P6_VIN2_AIN8	P6_DPD_PWR	50
51	P6_DPD_HPD	P4_P6_VIN1_AIN7	52
53	GND	GND	54
55	PMC_D_TMDSCN	PMC_D_TMDS0N	56
57	PMC_D_TMDSCP	PMC_D_TMDS0P	58
59	GND	GND	60
61	PMC_D_TMDS1N	PMC_D_TMDS2N	62
63	PMC_D_TMDS1P	PMC_D_TMDS2P	64

Note: # selected by RG_SEL switch set OFF.
Differential Pairs are shaded

Table 4-47 PMC Pn4 Connector, DVI Pinout (Mistral-BEL)

Pin	Signal Name	Signal Name	Pin
1	GND	PMC_D_DDCDAT	2
3	P4_P6_VIN2	PMC_D_DDCLK	4
5	n/c	GND	6
7	n/c	P6_DPF_PWR	8
9	P6_DPF_HPD	n/c	10
11	GND	GND	12
13	PMC_F_TMDSCN	PMC_F_TMDS0N	14
15	PMC_F_TMDSCP	PMC_F_TMDS0P	16
17	GND	GND	18
19	PMC_F_TMDS1N	PMC_F_TMDS2N	20
21	PMC_F_TMDS1P	PMC_F_TMDS2P	22
23	GND	P4_P6_VIN1	24
25	n/c	GND	26
27	n/c	n/c	28
29	GND	GND	30
31	n/c	n/c	32
33	n/c	n/c	34
35	GND	GND	36
37	n/c	n/c	38
39	n/c	n/c	40
41	GND	GND	42
43	n/c	PMC_F_DDCDAT	44
45	n/c	PMC_F_DDCLK	46
47	GND	GND	48
49	n/c	P6_DPD_PWR	50
51	P6_DPD_HPD	n/c	52
53	GND	GND	54
55	PMC_D_TMDSCN	PMC_D_TMDS0N	56
57	PMC_D_TMDSCP	PMC_D_TMDS0P	58
59	GND	GND	60
61	PMC_D_TMDS1N	PMC_D_TMDS2N	62
63	PMC_D_TMDS1P	PMC_D_TMDS2P	64

Note: Differential Pairs are shaded
n/c means user must not connect to pin – it may be active
Revised 22-Mar-2016 (corrected pin 5 – should be n/c)

4.13.1 Wirelist: MerlinPXC /2 PMC Pn4 to DisplayPort Channel C

Table 4-48 Merlin /2 PMC Pn4 to DisplayPort Channel C Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
31	PMC_DPC3N	12	MDPx3N	100Ω shielded, twisted pair
33	PMC_DPC3P	10	MDPx3P	100Ω shielded, twisted pair
35	GND	8	Ground	Ground
32	PMC_DPC2N	17	MDPx2N	100Ω shielded, twisted pair
34	PMC_DPC2P	15	MDPx2P	100Ω shielded, twisted pair
36	GND	13	Ground	Ground
37	PMC_DPC1N	11	MDPx1N	100Ω shielded, twisted pair
39	PMC_DPC1P	9	MDPx1P	100Ω shielded, twisted pair
41	GND	7	Ground	Ground
38	PMC_DPC0N	5	MDPx0N	100Ω shielded, twisted pair
40	PMC_DPC0P	3	MDPx0P	100Ω shielded, twisted pair
42	GND	1	Ground	Ground
25	P6_DPC_CEC #	6	MDPx_CEC	
27	P6_DPC_HPD	2	MDPx_HPD	
26	P6_DPC_PWR	20	MDPx_PWR	Stranded, 24ga min
28	P6_DPC_PIN13	4	MDPx_PIN13	
30	GND	19	GND_PWR	Stranded, 24ga min
43	PMC_DPC_AUXN #	18	MDPx_AUXN	100Ω shielded, twisted pair
45	PMC_DPC_AUXP #	16	MDPx_AUXP	100Ω shielded, twisted pair
47	GND #	14	Ground	Ground

selected by RG_SEL switch set OFF

4.13.2 Wirelist: MerlinPXC /2 PMC Pn4 to DisplayPort Channel D

Table 4-49 Merlin /2 PMC Pn4 to DisplayPort Channel D Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
55	PMC_DPD3N	12	MDPx3N	100Ω shielded, twisted pair
57	PMC_DPD3P	10	MDPx3P	100Ω shielded, twisted pair
59	GND +	8	Ground	Ground
56	PMC_DPD2N	17	MDPx2N	100Ω shielded, twisted pair
58	PMC_DPD2P	15	MDPx2P	100Ω shielded, twisted pair
60	GND *	13	Ground	Ground
61	PMC_DPD1N	11	MDPx1N	100Ω shielded, twisted pair
63	PMC_DPD1P	9	MDPx1P	100Ω shielded, twisted pair
59	GND +	7	Ground	Ground
62	PMC_DPD0N	5	MDPx0N	100Ω shielded, twisted pair
64	PMC_DPD0P	3	MDPx0P	100Ω shielded, twisted pair
60	GND *	1	Ground	Ground
49	P6_DPD_CEC	6	MDPx_CEC	
51	P6_DPD_HPD	2	MDPx_HPD	
50	P6_DPD_PWR	20	MDPx_PWR	Stranded, 24ga min
52	P6_DPD_PIN13	4	MDPx_PIN13	
54	GND	19	GND_PWR	Stranded, 24ga min
2	PMC_DPD_AUXN	18	MDPx_AUXN	100Ω shielded, twisted pair
4	PMC_DPD_AUXP	16	MDPx_AUXP	100Ω shielded, twisted pair
12	GND	14	Ground	Ground

+, * shared ground pin

4.13.3 Wirelist: Merlin /2 PMC Pn4 to DisplayPort Channel F

Table 4-50 Merlin /2 PMC Pn4 to DisplayPort Channel F Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
13	PMC_DPF3N	12	MDPx3N	100Ω shielded, twisted pair
15	PMC_DPF3P	10	MDPx3P	100Ω shielded, twisted pair
17	GND	8	Ground	Ground
14	PMC_DPF2N	17	MDPx2N	100Ω shielded, twisted pair
16	PMC_DPF2P	15	MDPx2P	100Ω shielded, twisted pair
18	GND	13	Ground	Ground
19	PMC_DPF1N	11	MDPx1N	100Ω shielded, twisted pair
21	PMC_DPF1P	9	MDPx1P	100Ω shielded, twisted pair
23	GND	7	Ground	Ground
20	PMC_DPF0N	5	MDPx0N	100Ω shielded, twisted pair
22	PMC_DPF0P	3	MDPx0P	100Ω shielded, twisted pair
24	GND	1	Ground	Ground
7	P6_DPF_CEC #	6	MDPx_CEC	
9	P6_DPF_HPD	2	MDPx_HPD	
8	P6_DPF_PWR	20	MDPx_PWR	Stranded, 24ga min
10	P6_DPF_PIN13	4	MDPx_PIN13	
12	GND	19	GND_PWR	Stranded, 24ga min
44	PMC_DPF_AUXN #	18	MDPx_AUXN	100Ω shielded, twisted pair
46	PMC_DPF_AUXP #	16	MDPx_AUXP	100Ω shielded, twisted pair
48	GND #	14	Ground	Ground

selected by RG_SEL switch set OFF

4.13.4 Wirelist: Merlin /2 PMC Pn4 to USB

Table 4-51 Merlin /2 PMC Pn4 to USB Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	USB Pin	USB Name	Cable Type
5	P4_USB_V	1	Switched Power (3.3V)	Stranded, 24ga min
1	PMC_USB_2_DN	2	USB 2.0 DATAN	100Ω shielded, twisted pair
3	PMC_USB_2_DP	3	USB 2.0 DATAP	100Ω shielded, twisted pair
11	GND	5	Ground	Ground

4.13.5 Wirelist: Merlin /1R PMC Pn4 to RG-101 VGA

Table 4-52 Merlin /1R PMC Pn4 to RG-101 VGA Wirelist

Pn4 Pin	Pn4 Name	VGA Pin	VGA Name	Cable Type
46	R_DAC1_FN_R +	1	Red	75Ω Coax, pin 6 Ground
47	G_DAC1_FN_R +	2	Green	75Ω Coax, pin 7 Ground
48	B_DAC1_FN_R +	3	Blue	75Ω Coax, pin 8 Ground
45	GND	5-8, 10, 11	Ground	Ground
6	P4_F5V *	9	Fused +5 Volts, .25A max	5V for DDC, 24ga stranded
25	DDCDATA_DAC1 +, *	12	DDCDA	Twisted Pair, pin 10 Ground
43	HS_DAC1_RN_R +	13	HSYNC	Twisted Pair, pin 5 Ground
44	VS_DAC1_RN_R +	14	VSYNC	Twisted Pair, pin 5 Ground
7	DDCCLK_DAC1 +, *	15	DDCCK	Twisted Pair, pin 10 Ground

+ selected by RG_SEL switch set ON

* enhancement to standard RG-101 pinout

4.13.6 Wirelist: Merlin /3 PMC Pn4 to BNC Video Input Connectors

Table 4-53 Wirelist: Merlin /3 PMC Pn4 to BNC Video Input Connectors

Pn4 Pin	Pn4 Name	BNC Connector Pin	BNC Cable Name	Cable Type
24	P4_P6_VIN7	1	VIN8	75Ω coax
26	GND	2		Ground
3	P4_P6_VIN8	1	VIN7	75Ω coax
5	GND	2		Ground
10	P4_P6_VIN5	1	VIN5	75Ω coax
11	GND	2		Ground
7	P4_P6_VIN6	1	VIN6	75Ω coax
11	GND	2		Ground
52	P4_P6_VIN1_AIN7 *	1	VIN1 or AIN7 *	75Ω/50Ω coax
48	GND	2		Ground
49	P4_P6_VIN2_AIN8 *	1	VIN2 or AIN8 *	75Ω/50Ω coax
47	GND	2		Ground

* Shared Video/Audio Input. Build option determines VINx or AINx

Use 75Ω coax for video, 50Ω coax for Audio

4.13.7 Wirelist: Merlin /3 PMC Pn4 to DisplayPort Channel C

Table 4-54 Merlin /3 PMC Pn4 to DisplayPort Channel C Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire

Pn4 Pin	Pn4 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
31	PMC_DPC3N	12	MDPx3N	100Ω shielded, twisted pair
33	PMC_DPC3P	10	MDPx3P	100Ω shielded, twisted pair
35	GND	8	Ground	Ground
32	PMC_DPC2N	17	MDPx2N	100Ω shielded, twisted pair
34	PMC_DPC2P	15	MDPx2P	100Ω shielded, twisted pair
36	GND	13	Ground	Ground
37	PMC_DPC1N	11	MDPx1N	100Ω shielded, twisted pair
39	PMC_DPC1P	9	MDPx1P	100Ω shielded, twisted pair
41	GND	7	Ground	Ground
38	PMC_DPC0N	5	MDPx0N	100Ω shielded, twisted pair
40	PMC_DPC0P	3	MDPx0P	100Ω shielded, twisted pair
42	GND	1	Ground	Ground
25	P6_DPC_CEC +	6	MDPx_CEC	
27	P6_DPC_HPD	2	MDPx_HPD	
1	P6_DPC_PWR	20	MDPx_PWR	Stranded, 24ga min
28	P6_DPC_PIN13	4	MDPx_PIN13	
5	GND	19	GND_PWR	Stranded, 24ga min
43	PMC_DPC_AUXN +	18	MDPx_AUXN	100Ω shielded, twisted pair
45	PMC_DPC_AUXP +	16	MDPx_AUXP	100Ω shielded, twisted pair
47	GND	14	Ground	Ground

+ selected by RG_SEL switch set OFF

Differential Pairs are shaded

4.13.8 Wirelist: Merlin /3 PMC Pn4 to DVI Channel D

Table 4-55 Merlin /3 PMC Pn4 to DVI Channel D Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	DVI Pin	DVI Name	Cable Type
55	PMC_D_TMDSCN	24	TMDS CLK-	100Ω shielded, twisted pair
57	PMC_D_TMDSCP	23	TMDS CLK+	100Ω shielded, twisted pair
53	GND	22	Ground	Ground
56	PMC_D_TMDS0N	17	TMDS Data0-	100Ω shielded, twisted pair
58	PMC_D_TMDS0P	18	TMDS Data0+	100Ω shielded, twisted pair
54	GND	19	Ground	Ground
61	PMC_D_TMDS1N	9	TMDS Data1-	100Ω shielded, twisted pair
63	PMC_D_TMDS1P	10	TMDS Data1+	100Ω shielded, twisted pair
59	GND	11	Ground	Ground
62	PMC_D_TMDS2N	1	TMDS Data2-	100Ω shielded, twisted pair
64	PMC_D_TMDS2P	2	TMDS Data2+	100Ω shielded, twisted pair
60	GND	3 +	Ground	Ground
51	P6_DPD_HPD	16	MDPx_HPD	
50	P6_DPD_PWR	14	+5 Power	Stranded, 24ga min
48	GND	15	GND_PWR	Stranded, 24ga min
5	GND	3 +		Ground for twisted pairs
2	PMC_D_DDCDAT	7	DDC Data	twisted pair w/ground
4	PMC_D_DDCCLK	6	DDC Clock	twisted pair w/ground

+ shared ground pin

Differential Pairs are shaded

4.13.9 Wirelist: Merlin /3 PMC Pn4 to DVI Channel F

Table 4-56 Merlin /3 PMC Pn4 to DVI Channel F Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	DVI Pin	DVI Name	Cable Type
13	PMC_F_TMDSCN	24	TMDS CLK-	100Ω shielded, twisted pair
15	PMC_F_TMDSCP	23	TMDS CLK+	100Ω shielded, twisted pair
11	GND	22	Ground	Ground
14	PMC_F_TMDS0N	17	TMDS Data0-	100Ω shielded, twisted pair
16	PMC_F_TMDSC0P	18	TMDS Data0+	100Ω shielded, twisted pair
12	GND	19	Ground	Ground
19	PMC_F_TMDS1N	9	TMDS Data1-	100Ω shielded, twisted pair
21	PMC_F_TMDS1P	10	TMDS Data1+	100Ω shielded, twisted pair
17	GND	11	Ground	Ground
20	PMC_F_TMDS2N	1	TMDS Data2-	100Ω shielded, twisted pair
22	PMC_F_TMDS2P	2	TMDS Data2+	100Ω shielded, twisted pair
18	GND	3 +	Ground	Ground
9	P6_DPF_HPD	16	MDPx_HPD	
8	P6_DPF_PWR	14	+5 Power	Stranded, 24ga min
6	GND	15	GND_PWR	Stranded, 24ga min
42	GND	3 +		Ground for twisted pairs
44	PMC_F_DDCDAT	7	DDC Data	twisted pair w/ground
46	PMC_F_DDCCLK	6	DDC Clock	twisted pair w/ground

+ shared ground pin

Differential Pairs are shaded

4.14 Merlin XMC Pn6 Connector and Wirelists

Table 4-57 XMC Pn6 Rear Panel Signal Definitions for Merlin

Schematic Name	Function
P4_USB_x	USB 2.0 Data, USB 3.0 Data
P4_USB_V	Switched 5V for USB. Use at least 24ga wire.
P6_F5V	Fused 5V for VGA. Use at least 24ga wire.
XMC_DPCxx	DisplayPort Ch C. 100Ω shielded, twisted pair
P6_DPC_AUXn	DisplayPort Ch C Control.. 100Ω shielded, twisted pair
P6_DPC_x	DisplayPort Ch C Auxiliary Signals: PWR, PIN13, HPD, CEC
XMC_DPDxx	DisplayPort Ch D. 100Ω shielded, twisted pair
P6_DPD_AUXn	DisplayPort Ch D Control.. 100Ω shielded, twisted pair
P6_DPD_x	DisplayPort Ch D Auxiliary Signals: PWR, PIN13, HPD, CEC
XMC_DPFxx	DisplayPort Ch F. 100Ω shielded, twisted pair
P6_DPF_AUXn	DisplayPort Ch F Control.. 100Ω shielded, twisted pair
P6_DPF_x	DisplayPort Ch F Auxiliary Signals: PWR, PIN13, HPD, CEC
R_DAC1_FN_R	VGA Red
G_DAC1_FN_R	VGA Green
B_DAC1_FN_R	VGA Blue
HS_DAC1_RN_R	VGA HSYNC
VS_DAC1_RN_R	VGA VSYNC
DDCCLK_DAC1	VGA DDCCK
DDCDATA_DAC1	VGA DDCDA
VGA Notes	
Red, Green, and Blue must use 75Ω coax. Each shield must be separately tied to ground. HSYNC and VSYNC should also use 75Ω coax.. DDCCK and DDCDA should each be twisted pairs with ground.	

Table 4-58 XMC Pn6 Connector (MerlinPXC/2 versions)

Position	A	B	C	D	E	F
1	P4_USB_DP	P4_USB_DN	GND	P4_USB_SSTXP	P4_USB_SSTXN	n/c
2	GND	GND	P6_F5V	GND	GND	GND
3	P4_USB_V	P4_USB_V	GND	P4_USB_SSRXP	P4_USB_SSRXN	n/c
4	GND	GND	P6_DPF_PWR	GND	GND	GND
5	XMC_DPF2P	XMC_DPF2N	P6_DPF_CEC	XMC_DPF3P	XMC_DPF3N	n/c
6	GND	GND	P6_DPF_PIN13	GND	GND	GND
7	XMC_DPF0P	XMC_DPF0N	P6_DPF_HPD	XMC_DPF1P	XMC_DPF1N	R_DAC1_FN_R
8	GND	GND	GND	GND	GND	GND
9	XMC_DPD_AUXP	XMC_DPD_AUXN	GND	n/c	n/c	G_DAC1_FN_R
10	GND	GND	P6_DPC_PWR	GND	GND	GND
11	XMC_DPC2P	XMC_DPC2N	P6_DPC_CEC	XMC_DPC3P	XMC_DPC3N	B_DAC1_FN_R
12	GND	GND	P6_DPC_PIN13	GND	GND	GND
13	XMC_DPC0P	XMC_DPC0N	P6_DPC_HPD	XMC_DPC1P	XMC_DPC1N	DDCDATA_DAC1
14	GND	GND	GND	GND	GND	GND
15	XMC_DPF_AUXP	XMC_DPF_AUXN	GND	XMC_DPC_AUXP	XMC_DPC_AUXN	HS_DAC1_RN_R
16	GND	GND	P6_DPD_PWR	GND	GND	GND
17	XMC_DPD2P	XMC_DPD2N	P6_DPD_CEC	XMC_DPD3P	XMC_DPD3N	VS_DAC1_RN_R
18	GND	GND	P6_DPD_PIN13	GND	GND	GND
19	XMC_DPD0P	XMC_DPD0N	P6_DPD_HPD	XMC_DPD1P	XMC_DPD1N	DDCCLK_DAC1

Note: n/c means no connect – user should not connect to the pin.
P4_USB_V & P6_F5V = 5V
Differential Pairs are shaded

Table 4-59 XMC Pn6 Connector (MerlinPXC/1x versions)

Position	A	B	C	D	E	F
1	n/c	n/c	GND	n/c	n/c	n/c
2	GND	GND	P6_F5V	GND	GND	GND
3	n/c	n/c	GND	n/c	n/c	n/c
4	GND	GND	P6_DPF_PWR	GND	GND	GND
5	XMC_DPF2P	XMC_DPF2N	P6_DPF_CEC	XMC_DPF3P	XMC_DPF3N	n/c
6	GND	GND	P6_DPF_PIN13	GND	GND	GND
7	XMC_DPF0P	XMC_DPF0N	P6_DPF_HPD	XMC_DPF1P	XMC_DPF1N	n/c
8	GND	GND	GND	GND	GND	GND
9	XMC_DPD_AUXP	XMC_DPD_AUXN	GND	n/c	n/c	n/c
10	GND	GND	P6_DPC_PWR	GND	GND	GND
11	XMC_DPC2P	XMC_DPC2N	P6_DPC_CEC	XMC_DPC3P	XMC_DPC3N	n/c
12	GND	GND	P6_DPC_PIN13	GND	GND	GND
13	XMC_DPC0P	XMC_DPC0N	P6_DPC_HPD	XMC_DPC1P	XMC_DPC1N	n/c
14	GND	GND	GND	GND	GND	GND
15	XMC_DPF_AUXP	XMC_DPF_AUXN	GND	XMC_DPC_AUXP	XMC_DPC_AUXN	n/c
16	GND	GND	P6_DPD_PWR	GND	GND	GND
17	XMC_DPD2P	XMC_DPD2N	P6_DPD_CEC	XMC_DPD3P	XMC_DPD3N	n/c
18	GND	GND	P6_DPD_PIN13	GND	GND	GND
19	XMC_DPD0P	XMC_DPD0N	P6_DPD_HPD	XMC_DPD1P	XMC_DPD1N	n/c

Note: n/c means no connect – user should not connect to the pin.
P6_F5V = 5V
Differential Pairs are shaded

4.14.1 Wirelist: Merlin /2 XMC Pn6 to DisplayPort Channel C

Table 4-60 Merlin PMC Pn6 to DisplayPort Channel C Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn6 Pin	Pn6 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
E11	XMC_DPC3N	12	MDPx3N	100Ω shielded, twisted pair
D11	XMC_DPC3P	10	MDPx3P	100Ω shielded, twisted pair
D10	GND	8	Ground	Ground
B11	XMC_DPC2N	17	MDPx2N	100Ω shielded, twisted pair
A11	XMC_DPC2P	15	MDPx2P	100Ω shielded, twisted pair
A10	GND	13	Ground	Ground
E13	XMC_DPC1N	11	MDPx1N	100Ω shielded, twisted pair
D13	XMC_DPC1P	9	MDPx1P	100Ω shielded, twisted pair
D12	GND	7	Ground	Ground
B13	XMC_DPC0N	5	MDPx0N	100Ω shielded, twisted pair
A13	XMC_DPC0P	3	MDPx0P	100Ω shielded, twisted pair
A12	GND	1	Ground	Ground
C11	P6_DPC_CEC	6	MDPx_CEC	
C13	P6_DPC_HPD	2	MDPx_HPD	
C10	P6_DPC_PWR	20	MDPx_PWR	Stranded, 24ga min
C12	P6_DPC_PIN13	4	MDPx_PIN13	
C9	GND	19	GND_PWR	Stranded, 24ga min
E15	XMC_DPC_AUXN	18	MDPx_AUXN	100Ω shielded, twisted pair
D15	XMC_DPC_AUXP	16	MDPx_AUXP	100Ω shielded, twisted pair
D14	GND	14	Ground	Ground

4.14.2 Wirelist: Merlin /2 XMC Pn6 to DisplayPort Channel D

Table 4-61 Merlin XMC Pn6 to DisplayPort Channel D Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn6 Pin	Pn6 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
E17	XMC_DPD3N	12	MDPx3N	100Ω shielded, twisted pair
D17	XMC_DPD3P	10	MDPx3P	100Ω shielded, twisted pair
D16	GND	8	Ground	Ground
B17	XMC_DPD2N	17	MDPx2N	100Ω shielded, twisted pair
A17	XMC_DPD2P	15	MDPx2P	100Ω shielded, twisted pair
A16	GND	13	Ground	Ground
E19	XMC_DPD1N	11	MDPx1N	100Ω shielded, twisted pair
D19	XMC_DPD1P	9	MDPx1P	100Ω shielded, twisted pair
D18	GND	7	Ground	Ground
B19	XMC_DPD0N	5	MDPx0N	100Ω shielded, twisted pair
A19	XMC_DPD0P	3	MDPx0P	100Ω shielded, twisted pair
A18	GND	1	Ground	Ground
C17	P6_DPD_CEC	6	MDPx_CEC	
C19	P6_DPD_HPD	2	MDPx_HPD	
C16	P6_DPD_PWR	20	MDPx_PWR	Stranded, 24ga min
C18	P6_DPD_PIN13	4	MDPx_PIN13	
C15	GND	19	GND_PWR	Stranded, 24ga min
B9	XMC_DPD_AUXN	18	MDPx_AUXN	100Ω shielded, twisted pair
A9	XMC_DPD_AUXP	16	MDPx_AUXP	100Ω shielded, twisted pair
A8	GND	14	Ground	Ground

4.14.3 Wirelist: Merlin /2 XMC Pn6 to DisplayPort Channel F

Table 4-62 Merlin XMC Pn6 to DisplayPort Channel F Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn6 Pin	Pn6 Name	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
E5	XMC_DPF3N	12	MDPx3N	100Ω shielded, twisted pair
D5	XMC_DPF3P	10	MDPx3P	100Ω shielded, twisted pair
D4	GND	8	Ground	Ground
B5	XMC_DPF2N	17	MDPx2N	100Ω shielded, twisted pair
A5	XMC_DPF2P	15	MDPx2P	100Ω shielded, twisted pair
A4	GND	13	Ground	Ground
E7	XMC_DPF1N	11	MDPx1N	100Ω shielded, twisted pair
D7	XMC_DPF1P	9	MDPx1P	100Ω shielded, twisted pair
D6	GND	7	Ground	Ground
B7	XMC_DPF0N	5	MDPx0N	100Ω shielded, twisted pair
A7	XMC_DPF0P	3	MDPx0P	100Ω shielded, twisted pair
A6	GND	1	Ground	Ground
C5	P6_DPF_CEC	6	MDPx_CEC	
C7	P6_DPF_HPD	2	MDPx_HPD	
C4	P6_DPF_PWR	20	MDPx_PWR	Stranded, 24ga min
C6	P6_DPF_PIN13	4	MDPx_PIN13	
C3	GND	19	GND_PWR	Stranded, 24ga min
B15	XMC_DPF_AUXN	18	MDPx_AUXN	100Ω shielded, twisted pair
A15	XMC_DPF_AUXP	16	MDPx_AUXP	100Ω shielded, twisted pair
A14	GND	14	Ground	Ground

4.14.4 Wirelist: Merlin /2 XMC Pn6 to USB

Table 4-63 Merlin XMC Pn6 to USB Wirelist

Each "L" wire in a data pair MUST be the same length as the "H" wire.

Pn6 Pin	Pn6 Name	USB Pin	USB Name	Cable Type
A3	P4_USB_V	1	Switched Power (3.3V)	Stranded, 24ga min
B1	XMC_USB_2_DN	2	USB 2.0 Data N	100Ω shielded, twisted pair
A1	XMC_USB_2_DP	3	USB 2.0 DataP	100Ω shielded, twisted pair
A2	GND	5	Power Ground	Power Ground
E1	P4_USB_SSTXN	6	USB 3.0 SS_TXN	100Ω shielded, twisted pair
D1	P4_USB_SSTXP	7	USB 3.0 SS_TXP	100Ω shielded, twisted pair
D2	GND	8	SS_Ground_Drain	SS_Ground_Drain
E3	P4_USB_SSRXN	9	USB 3.0 SS_RXN	100Ω shielded, twisted pair
D3	P4_USB_SSRXP	10	USB 3.0 SS_RXP	100Ω shielded, twisted pair

4.14.5 Wirelist: Merlin /2 XMC Pn6 to VGA

Table 4-64 Merlin XMC Pn4 to VGA Wirelist

Pn6 Pin	Pn4 Name	VGA Pin	VGA Name	Cable Type
F7	R_DAC1_FN_R	1	Red	75Ω Coax, pin 6 Ground
F9	G_DAC1_FN_R	2	Green	75Ω Coax, pin 7 Ground
F11	B_DAC1_FN_R	3	Blue	75Ω Coax, pin 8 Ground
F14	GND	5	DDC Ground	
F8	GND	6	Red Ground	
F10	GND	7	Green Ground	
F12	GND	8	Blue Ground	
C2	P6_F5V	9	Fused +5 Volts, .25A max	
F16	GND	10	Sync Ground	
C1	GND	11	Ground	
F13	DDCDATA_DAC1	12	DDCDA	Twisted Pair, pin 5 Ground
F15	HS_DAC1_RN_R	13	HSYNC	75Ω Coax, pin 10 Ground
F17	VS_DAC1_RN_R	14	VSYNC	75Ω Coax, pin 10 Ground
F19	DDCCLK_DAC1	15	DDCCK	Twisted Pair, pin 5 Ground

4.15 MerlinMTX PMC Pn4 Connector and Wirelists

Table 4-65 PMC Pn4 Rear Panel Signal Definitions for MerlinMTX

Schematic Name	Function
P4_ VINx	NTSC/PAL Video In
P4_VINx_AINx	Shared Video/Audio Input. Build option determines VINx or AINx
P4_F5V	Fused 5V for VGA. Use at least 24ga wire.
PMC_DPCxx	DisplayPort Ch C Data. 100Ω shielded, twisted pair
PMC_DPC_AUXx	DisplayPort Ch C AUX. 100Ω shielded, twisted pair
PMC_DPC_x	DisplayPort Ch C Control Signals: PWR, PIN13, HPD, CEC
PMC_TXxx_D	DVI Ch D. 100Ω shielded, twisted pair
PMC_D_DDCxxx	DVI Ch D Control. 100Ω shielded, each DDC paired with ground
P4_DPD_x	DVI Ch D Auxiliary Signals: PWR, HPD
PMC_TXxx_F	DVI Ch F. 100Ω shielded, twisted pair
PMC_F_DDCxxx	DVI Ch F Control. 100Ω shielded, each DDC paired with ground
P4_DPF_x	DVI Ch F Auxiliary Signals: PWR, HPD

Schematic Name	DVI/DP Mode	DVI Mode (Mistral-BEL)
P4_DPF_CEC_VIN7_AIN7	P4_DPF_CEC_VIN7_AIN7	n/c
P4_DPD_CEC_VIN8_AIN8	P4_DPD_CEC_VIN8_AIN8	n/c

Table 4-66 PMC Pn4 Connector, DVI/DP Pinout (MerlinMTX)

Pin	Signal Name	Signal Name	Pin
1	P4_DPC_PWR	PMC_D_DDCDAT	2
3	P4_VIN2	PMC_D_DDCLK	4
5	GND	GND	6
7	P4_DPF_CEC_VIN7_AIN7	P4_DPF_PWR	8
9	P4_DPF_HPD	P4_DPF_PIN13	10
11	GND	GND	12
13	PMC_F_TMDSCN	PMC_F_TMDS0N	14
15	PMC_F_TMDSCP	PMC_F_TMDS0P	16
17	GND	GND	18
19	PMC_F_TMDS1N	PMC_F_TMDS2N	20
21	PMC_F_TMDS1P	PMC_F_TMDS2P	22
23	GND	P4_VIN1	24
25	P4_DPC_CEC	GND	26
27	P4_DPC_HPD	P4_DPC_PIN13	28
29	GND	GND	30
31	PMC_DPC3N	PMC_DPC2N	32
33	PMC_DPC3P	PMC_DPC2P	34
35	GND	GND	36
37	PMC_DPC1N	PMC_DPC0N	38
39	PMC_DPC1P	PMC_DPC0P	40
41	GND	GND	42
43	PMC_DPC_AUXN	PMC_F_DDCDAT	44
45	PMC_DPC_AUXP	PMC_F_DDCLK	46
47	GND	GND	48
49	P4_DPD_CEC_VIN8_AIN8	P4_DPD_PWR	50
51	P4_DPD_HPD	P4_DPD_PIN13	52
53	GND	GND	54
55	PMC_D_TMDSCN	PMC_D_TMDS0N	56
57	PMC_D_TMDSCP	PMC_D_TMDS0P	58
59	GND	GND	60
61	PMC_D_TMDS1N	PMC_D_TMDS2N	62
63	PMC_D_TMDS1P	PMC_D_TMDS2P	64

Note: Differential Pairs are shaded

Table 4-67 PMC Pn4 Connector, DVI Pinout (Mistral-BEL)

Pin	Signal Name	Signal Name	Pin
1	GND	PMC_D_DDCDAT	2
3	P4_VIN2	PMC_D_DDCLK	4
5	n/c	GND	6
7	n/c	P4_DPF_PWR	8
9	P4_DPF_HPD	n/c	10
11	GND	GND	12
13	PMC_F_TMDSCN	PMC_F_TMDS0N	14
15	PMC_F_TMDSCP	PMC_F_TMDS0P	16
17	GND	GND	18
19	PMC_F_TMDS1N	PMC_F_TMDS2N	20
21	PMC_F_TMDS1P	PMC_F_TMDS2P	22
23	GND	P4_VIN1	24
25	n/c	GND	26
27	n/c	n/c	28
29	GND	GND	30
31	n/c	n/c	32
33	n/c	n/c	34
35	GND	GND	36
37	n/c	n/c	38
39	n/c	n/c	40
41	GND	GND	42
43	n/c	PMC_F_DDCDAT	44
45	n/c	PMC_F_DDCLK	46
47	GND	GND	48
49	n/c	P4_DPD_PWR	50
51	P4_DPD_HPD	n/c	52
53	GND	GND	54
55	PMC_D_TMDSCN	PMC_D_TMDS0N	56
57	PMC_D_TMDSCP	PMC_D_TMDS0P	58
59	GND	GND	60
61	PMC_D_TMDS1N	PMC_D_TMDS2N	62
63	PMC_D_TMDS1P	PMC_D_TMDS2P	64

Note: Differential Pairs are shaded
n/c means user must not connect to pin – it may be active

4.15.1 Wirelist: MerlinMTX PMC Pn4 to BNC Video Input Connectors

Table 4-68 Wirelist: MerlinMTX PMC Pn4 to BNC Video Input Connectors

Pn4 Pin	Pn4 Name	BNC Connector Pin	BEL-Mistral?	BNC Cable Name	Cable Type
24	P4_VIN1	1	Yes	VIN1	75Ω coax
26	GND	2			Ground
3	P4_VIN2	1	Yes	VIN2	75Ω coax
5	GND+	2			Ground
7	P4_VIN7_AIN7*	1	No	VIN7 or AIN7*	75Ω/50Ω coax
5	GND+	2			Ground
49	P4_VIN8_AIN8*	1	No	VIN8 or AIN8*	75Ω/50Ω coax
47	GND	2			Ground

\+ shared ground pin

* Shared Video/Audio Input. Build option determines VINx or AINx

Use 75Ω coax for video, 50Ω coax for Audio

4.15.2 Wirelist: MerlinMTX PMC Pn4 to DisplayPort Channel C

Table 4-69 MerlinMTX PMC Pn4 to DisplayPort Channel C Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire

Pn4 Pin	Pn4 Name	BEL-Mistral?	Mini DisplayPort Pin	Mini DisplayPort Name	Cable Type
31	PMC_DPC3N	No	12	MDPx3N	100Ω shielded, twisted pair
33	PMC_DPC3P		10	MDPx3P	100Ω shielded, twisted pair
35	GND		8	Ground	Ground
32	PMC_DPC2N		17	MDPx2N	100Ω shielded, twisted pair
34	PMC_DPC2P		15	MDPx2P	100Ω shielded, twisted pair
36	GND		13	Ground	Ground
37	PMC_DPC1N		11	MDPx1N	100Ω shielded, twisted pair
39	PMC_DPC1P		9	MDPx1P	100Ω shielded, twisted pair
41	GND		7	Ground	Ground
38	PMC_DPC0N		5	MDPx0N	100Ω shielded, twisted pair
40	PMC_DPC0P		3	MDPx0P	100Ω shielded, twisted pair
42	GND		1	Ground	Ground
25	P4_DPC_CEC		6	MDPx_CEC	
27	P4_DPC_HPD		2	MDPx_HPD	
1	P4_DPC_PWR		20	MDPx_PWR	Stranded, 24ga min
28	P4_DPC_PIN13		4	MDPx_PIN13	
5	GND		19	GND_PWR	Stranded, 24ga min
43	PMC_DPC_AUXN		18	MDPx_AUXN	100Ω shielded, twisted pair
45	PMC_DPC_AUXP		16	MDPx_AUXP	100Ω shielded, twisted pair
47	GND		14	Ground	Ground

Differential Pairs are shaded

4.15.3 Wirelist: MerlinMTX PMC Pn4 to DVI Channel D

Table 4-70 MerlinMTX PMC Pn4 to DVI Channel D Wirelist

Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	BEL-Mistral?	DVI Pin	DVI Name	Cable Type
55	PMC_D_TMDSCN	Yes	24	TMDS CLK-	100Ω shielded, twisted pair
57	PMC_D_TMDSCP		23	TMDS CLK+	100Ω shielded, twisted pair
53	GND		22	Ground	Ground
56	PMC_D_TMDS0N		17	TMDS Data0-	100Ω shielded, twisted pair
58	PMC_D_TMDS0P		18	TMDS Data0+	100Ω shielded, twisted pair
54	GND		19	Ground	Ground
61	PMC_D_TMDS1N		9	TMDS Data1-	100Ω shielded, twisted pair
63	PMC_D_TMDS1P		10	TMDS Data1+	100Ω shielded, twisted pair
59	GND		11	Ground	Ground
62	PMC_D_TMDS2N		1	TMDS Data2-	100Ω shielded, twisted pair
64	PMC_D_TMDS2P		2	TMDS Data2+	100Ω shielded, twisted pair
60	GND		3 +	Ground	Ground
51	P4_DPD_HPD		16	MDPx_HPD	
50	P4_DPD_PWR		14	+5 Power	Stranded, 24ga min
48	GND		15	GND_PWR	Stranded, 24ga min
5	GND		3 +	Ground	Ground for twisted pairs
2	PMC_D_DDCDAT		7	DDC Data	twisted pair w/ground
4	PMC_D_DDCCLK		6	DDC Clock	twisted pair w/ground

+ shared ground pin

Differential Pairs are shaded

4.15.4 Wirelist: MerlinMTX PMC Pn4 to DVI Channel F

Table 4-71 MerlinMTX PMC Pn4 to DVI Channel F Wirelist

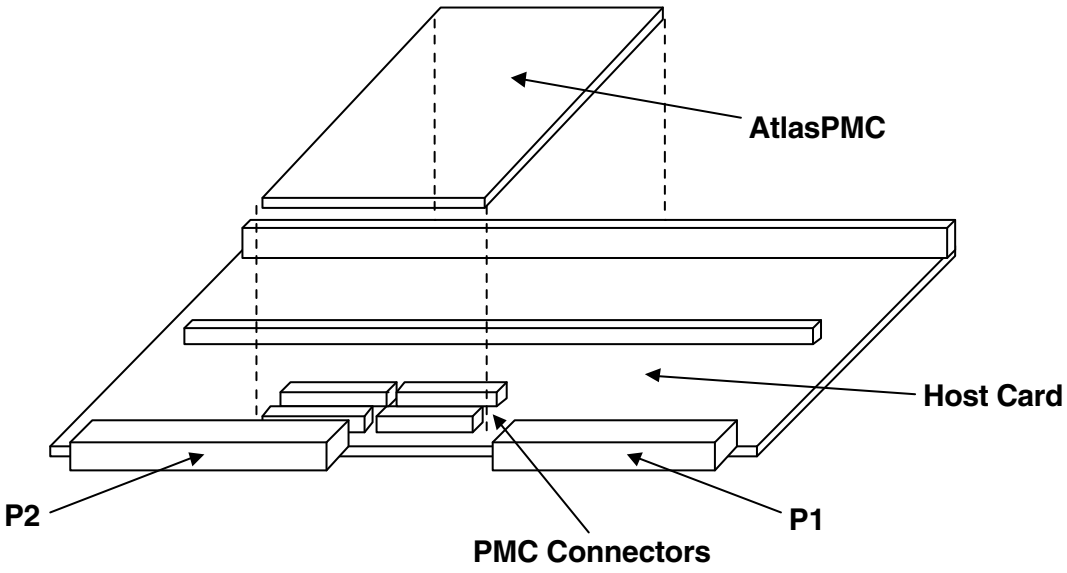
Each “L” wire in a data pair MUST be the same length as the “H” wire.

Pn4 Pin	Pn4 Name	BEL-Mistral?	DVI Pin	DVI Name	Cable Type
13	PMC_F_TMDSCN	Yes	24	TMDS CLK-	100Ω shielded, twisted pair
15	PMC_F_TMDSCP		23	TMDS CLK+	100Ω shielded, twisted pair
11	GND		22	Ground	Ground
14	PMC_F_TMDS0N		17	TMDS Data0-	100Ω shielded, twisted pair
16	PMC_F_TMDSC0P		18	TMDS Data0+	100Ω shielded, twisted pair
12	GND		19	Ground	Ground
19	PMC_F_TMDS1N		9	TMDS Data1-	100Ω shielded, twisted pair
21	PMC_F_TMDS1P		10	TMDS Data1+	100Ω shielded, twisted pair
17	GND		11	Ground	Ground
20	PMC_F_TMDS2N		1	TMDS Data2-	100Ω shielded, twisted pair
22	PMC_F_TMDS2P		2	TMDS Data2+	100Ω shielded, twisted pair
18	GND		3 +	Ground	Ground
9	P4_DPF_HPD		16	MDPx_HPD	
8	P4_DPF_PWR		14	+5 Power	Stranded, 24ga min
6	GND		15	GND_PWR	Stranded, 24ga min
42	GND		3 +	Ground	Ground for twisted pairs
44	PMC_F_DDCDAT		7	DDC Data	twisted pair w/ground
46	PMC_F_DDCCLK		6	DDC Clock	twisted pair w/ground

+ shared ground pin

Differential Pairs are shaded

Chapter 5
Installing Your Rastergraf Graphics Board



5.1 Introduction

There are several steps involved in getting your Rastergraf board to work in your system:

- Unpack the Rastergraf board.
- Review and perhaps change the switch settings on the board
- Install the Rastergraf board.
- Install the software – this is covered in Chapter 8.9**.**

This chapter shows you how to install the Rastergraf board in your computer. Your Rastergraf software User's Manual (e.g., SDL) provides instructions on how to install the software.

5.2 Special Considerations

5.2.1 Power Requirements

The Agate and Merlin are high-performance boards and as such, they use more power than many other mezzanine boards, although not more than comparable graphics boards from other vendors.

According to the original PMC specification, the board is not supposed to exceed 7.5W. Both the Agate and Merlin can easily exceed this limit, as do many other PMC and XMC boards.

The XMC specification (VITA 42) bases its power dissipation limits on what the current/power pin limit is. That is specified at 1A/pin, for a theoretical limit of about 100W.

The typical Agate or Merlin shouldn't run more than 25W to 30W when really exercised.

But, the point is that you must ensure that the CPU or carrier board that you plan to use doesn't enforce current limits on PMC or XMC locations. If it does, and it is less than 30W, you could have problems.

5.2.2 VPWR

One thing that is problematic about XMC is that the primary power supply pins, which are called VPWR, can present either 5V or 12V. This setting is usually not controllable by the user. It is set by the CPU or carrier designer. The VPWR voltage should be listed in the board specifications.

This variability in voltage specification is not a great idea because transients often occur on power up or down, and the voltage detection on the target board (i.e. Agate or Merlin) could make a mistake and expose the board to 12V when it thought it was going to be 5V. For this reason,

rather than allow the board to auto detect the voltage (which it certainly could do), a switch must be set to allow the board to power up with the right voltage. The switch and voltage observed don't match, the board won't start up

Rastergraf ALWAYS prefers 5V operation as there is less likelihood of something going wrong that would damage the graphics board power supplies. So, if you DO have a choice, please always choose 5V for VPWR.

5.2.3 Performance Requirement for the CX25858

As mentioned elsewhere in this manual, some PMC-based systems may not have sufficient bandwidth to support the Agate CX25858 digitizer.

It has been observed that the CX25858 8-channel video digitizer doesn't like low bandwidth PMC systems. Please make sure that your PMC system is at least 32-bit, 66MHz. Both 64-bit and a higher bus frequency are to be desired.

We have not seen problems with the graphics or USB chips. Nevertheless, a slow PMC system will never be able to deliver the performance you might hope to get from either the Agate or Merlin.

5.2.4 Power Supplies

Please be aware that for PMC systems, some older processors do not supply 3.3V to the PMC connectors. Both the Agate and Merlin REQUIRE 3.3V and 5.0V to operate correctly.

For XMC systems, both 3.3V and VPWR are required, and as mentioned above, please use VPWR=5V (not 12V) when you have a choice.

5.3 Unpacking Your Board

When you unpack your board, inspect the contents to see if any damage occurred in shipping. If there has been physical damage, file a claim with the carrier at once and contact Rastergraf for information regarding repair or replacement. Do not attempt to use damaged equipment.

Caution

Be careful not to remove the board from its antistatic bag until you are ready to install it. You should always were a grounded wrist strap whenever handling computer boards.

5.4 Preparing for Installation

The Agate and Merlin can be installed in hosts CPU or carrier boards that provide PMC and/or XMC mezzanine card sites.

While there is no mystery to getting access to board resources on the front panel, it is not always obvious what you can do with the rear I/O, if you need to use that. We have even seen CPU cards that install both XMC connectors but don't actually support XMC rear I/O.

Please look at Chapter 4, as it focuses on the rear I/O access issues. If that chapter isn't helpful, please don't hesitate to contact Rastergraf and we will try to help you.

5.4.1 Interrupt Settings

The boards use the PMC **INTA** interrupt request line for the particular slot it is plugged into. In some computers, each slot ***may*** map its local interrupt lines to a permuted set of INTA-INTD, which means that the board will show up on a different interrupt line according to the slot it is plugged into. The device driver will usually notice this and compensate for it. In any case, the user has no direct control (e.g., jumpers) over what interrupt line the graphics board will use.

5.4.2 Address Settings

Since the PCI or PCIe bus and the boards are configured by the Operating System (OS) and/or BIOS while booting up, there aren't any address jumpers. The address settings are programmable and are set up by the software as a result of information supplied by the OS at boot time. Refer to the Rastergraf software User's Manuals for more information.

The software sets up the BARs (Base Address Registers) and other relevant control registers in all of the PCI devices on the board. The Rastergraf device drivers will load the BARs if the OS or BIOS did not. If you can determine the actual PCI base address, you might even be able to probe the address spaces with an on-line debugger once the driver code has run.

The ability to probe the board is dependent on the CPU memory map as implemented by the system OS and the address ranges of the PCI or PCIe bus as determined by the CPU hardware. These things change from OS to OS, board-to-board, and vendor-to-vendor, making it a difficult task. Most likely, if you use Rastergraf supplied software, the board will show up and you will get pictures.

5.5 AgatePXC Switch Packs and Jumpers

The AgatePXC has 10 switch packs and 4 jumper positions. Where practical, switch packs were used because they are easier to use.

5.5.1 AgatePXC Switch Packs

SW1 (May not be installed)

Position	Settings	Default
SW1-1 thru SW1-8	Reserved	**Off**

SW2

Position	Settings	Default
SW2-1	BIOS ROM 0 Do not change.	**Off**
SW2-2	Spare, not used.	**Off**
SW2-3	Off: VPWR = 5V On: VPWR = 12V	**Off**
SW2-4 SW2-5	JTAG Loop Bypass Do not change.	**SW2-4 Off** **SW2-5 On**
SW2-6	Off: PMC runs in PCI-X 66/133 mode On: PMC runs in PCI mode	**Off**
SW2-7	Off: PMC runs in PCI-X/133 mode On: PMC runs in PCI-X/66 mode	**Off**
SW2-8	Enable Host JTAGRST Do not change.	**Off**

SW3

Position	Settings	Default
SW3-1	Off: RGBHV Input on Front Panel On: RGBHV Input on Pn4/Pn6	**Off**
SW3-2	Power Sequence Bypass Do not change.	**Off**

SW4

As explained in Chapter 2, it is possible to reduce the Agate's power consumption by forcing the host side and/or E4690 side of the 89HPES24T6G2 PCIe switch to use 4 lanes instead of 8. In most cases, x4 operation will not affect overall performance and it will reduce power consumption by several watts.

If you are running in a PMC host, then the Host Side PCIe bus is always x4 because the PI7C9X130 PCIe to PCI bridge is a x4, PCIe 1.1 device. But, the E4690 side could still be running x4 or x8. There is absolutely no reason to run it at x8 on a PMC host.

Position	Settings	Default
SW4-1	Off: Agate Host Side PCIe bus x4 On: Agate Host Side PCIe bus x8 ***Set to Off when running in a PMC system.***	**Off**
SW4-2	Off: Agate E4690 PCIe bus x4 On: Agate E4690 PCIe bus x8 ***Set to Off when running in a PMC system.***	**Off**

SW5

This is a small rectangular pushbutton that is used to restart the STM32F427 on-board control processor, the CX3 MIPI controller, and the FX3 analog video/DVI input controller.

After such a reset, the ST LED on the front panel should slowly turn off and on, the CX LED on the front panel should blink off and on about 1/s and the FX LED

If you are connected to a Hyperterminal window when you hit reset you will have to exit the program and restart because the USB handshaking in Windows gets confused.

Position	Settings	Default
SW5-1	Press pushbutton to reset STM32F427	**Off**

SW6

This is a small rectangular pushbutton that is used to toggle STM32F427 port bit PA_00. Pressing it will cause the Green, Yellow, and Red LEDs along the edge of the board (side 2) to light up in sequence.

Position	Settings	Default
SW6-1	Press pushbutton to toggle port bit PA_00	**Off**

SW7

Position	Settings	Default
SW7-1	Off: VGA Controller capability enabled On: Agate will not be recognized as the system's VGA controller	**Off**
SW7-2	Off: Normal system power control On: Request STM to reduce core voltage ***Function is not currently implemented.***	**Off**
SW7-3	Reserved Do not change.	**Off**
SW7-4	Reserved Do not change.	**Off**
SW7-5	Reserved Do not change.	**Off**
SW7-6	Reserved Do not change.	**Off**
SW7-7	Reserved Do not change.	**Off**
SW7-8	Standard master clock. Do not change.	**On**

SW8

Select FX3 boot mode to either be:

a) USB (boot directly using USB to obtain boot code from system OS

b) SPI (boot from local flash or if not present, boot from USB)

Settings			Default
SW8-2	**SW8-1**	**Boot Mode**	
On	Off	SPI, On Failure, USB	**selected**
Off	On	Always boot to USB	

SW9

SW9-2 controls BOOT0 on the STM.

OFF (BOOT0 = 0) selects firmware preprogrammed into STM flash;

ON (BOOT0 = 1) selects STM bootloader/DFU mode, which uses the STM FS port to access the device holding the image.

(BOOT1 set permanently to "0" with a 1K pulldown to ground)

Position	Settings	Default
SW9-1	Off: allow STM to CX25858 EEPROM. On: allow access only by OS based apps	**Off**
SW9-2	Off: STM runs from internal flash On: STM boots from external USB device (DFU Mode)	**Off**

SW10

Select CX3 boot mode to either be:

a) USB (boot directly using USB to obtain boot code from system OS

b) SPI (boot from local flash or if not present, boot from USB)

Settings			Default
SW10-2	**SW10-1**	**Boot Mode**	
On	Off	SPI, On Failure, USB	**selected**
Off	On	USB	

5.5.2 AgatePXC Jumpers

JP011D5

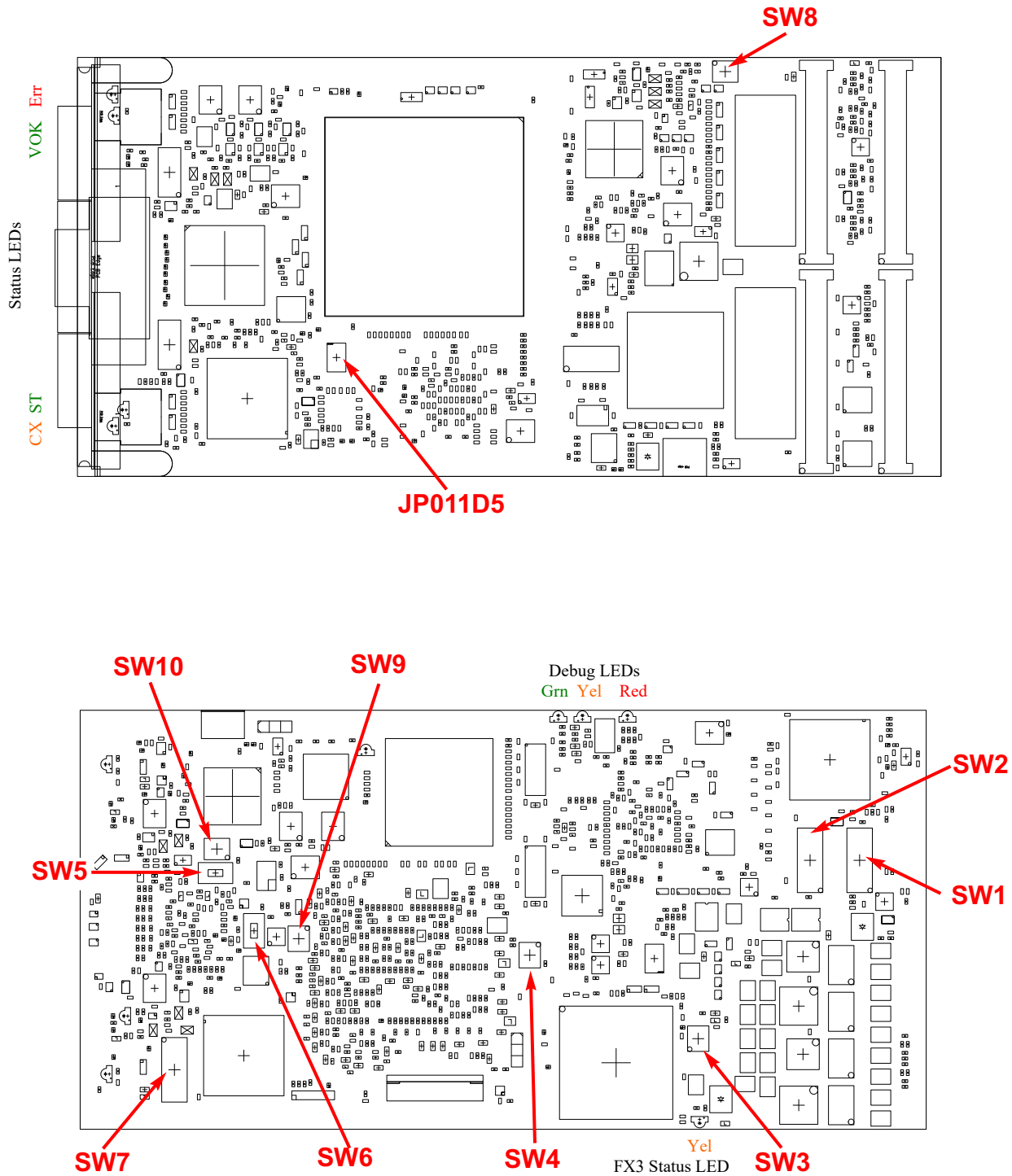
JP011D5 is used to select whether the STM OTG_FS port or the OTG_HS port is connected to Mini B USB connector J011D5.

Please see Section 3.9.2 for information about the connector and why you would want to choose one setting over another.

In the table below, the Red and Black refer to the color of the shunts used to make the connections. By convention, HS uses the Black shunts and FS uses Red shunts.

Function	Settings	Default
OTG_HS to J011D5 OTG_FS to uPD720201 Port 1	JP011D5 1-2, 5-6 (Black) JP011D5 3-4, 7-8 (Red)	**No** **No**
OTG_FS to J011D5 OTG_HS to uPD720201 Port 1	JP011D5 1-3, 5-7 (Red) JP011D5 2-4, 6-8 (Black)	**Yes** **Yes**

Figure 5-1 AgatePXC Switch Packs and Jumpers Locations



5.5.3 AgatePXC PIM Jumpers

JP011T2 and JP021T2

JP011T2 and JP021T2 are combined into one 2x8 array. They are used to select between RGBHV In or the Ch 1 VGA Out for certain pins on the AgatePXC PIM J011X4 50-pin Multi-Function Connector.

Due to space limitations, this same selection is not available on the AgatePXC itself.

Function	Settings			Default
RGBHV In on J011X4	JP011T2	1-3	Red	yes
	JP011T2	5-6	Black	yes
	JP011T2	7		
		to	Red	yes
	JP021T2	1		
	JP021T2	3-4	Black	yes
	JP021T2	5-7	Red	yes
VGA Ch 1 on J011X4	JP011T2	1-2	Red	no
	JP011T2	4-6	Black	no
	JP011T2	7-8	Red	no
	JP021T2	2-4	Black	no
	JP021T2	5-6	Red	no

JP011T4

JP011T4 selects between DAC2 DDCDA/DDCCL and Audio In Ch 7/8 on AgatePXC PIM J011X4 50-pin Multi-Function Connector.

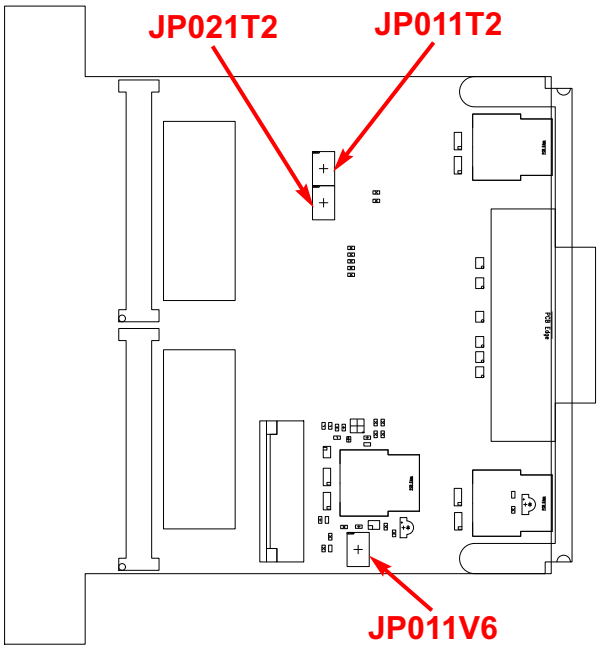
Function	Settings			Default
DDCDA	JP011T4	1-2	Red	no
DDCCL	JP011T4	5-6	Black	no
Audio Ch 7	JP011T4	3-4	Red	yes
Audio Ch 8	JP011T4	7-8	Black	yes

JP011V6

JP011V6 is used to control pins on the WandCam paddleboard.

Function		Settings			Default
PDW_XCLK_R	24MHz Clock Source	JP011T4	1-2	Red	yes
PDW_XCLK_J	Clock input to camera				
PDW_PDN	Tied to pulldown to prevent camera from going into power down. Do not use – testing only				
PDW_XRST_L	10K/0.1uf RC to make a simple reset	JP011T4	3-5	Black	no
PDW_XRST_J	Reset input to camera				
PDW_XRST	Possible reset source form host. If it exists, use instead of PDW_XRST_L	JP011T4	5-6	Red	no
-	Not used	JP011T4	7, 8	-	-

Figure 5-2 AgatePXC PIM Jumper Locations



5.6 MerlinPXC Switch Packs and Jumpers

The MerlinPXC has 8 switch packs and 4 jumper positions. Where practical, switch packs were used because they are easier to use.

5.6.1 MerlinPXC Switch Packs

SW1 (May not be installed)

Position	Settings	Default
SW1-1	VGA on PMC Pn4 Rear I/O connector. When selected, DP Ch C and Ch F are unusable. DP Ch D remains. On: VGA mode is NOT selected	**On**
SW1-2 thru SW1-8	Reserved	**Off**

SW2

Position	Settings	Default
SW2-1	Off: BIOS 0 Do not change.	**Off**
SW2-2	Spare, not used.	**Off**
SW2-3	Off: VPWR = 5V On: VPWR = 12V	**Off**
SW2-4 SW2-5	JTAG Loop Bypass Do not change.	**SW2-4 Off** **SW2-5 On**
SW2-6	Off: PMC runs in PCI-X 66/133 mode On: PMC runs in PCI mode	**Off**
SW2-7	Off: PMC runs in PCI-X/133 mode On: PMC runs in PCI-X/66 mode	**Off**
SW2-8	Enable Host JTAGRST Do not change.	**Off**

SW3

Position	Settings	Default
SW3-1	Off: DisplayPorts C/D/F on PMC Pn4 On: DisplayPorts C/D/F on XMC Pn6 But, see also SW7-3	**Of**
SW3-2	Power Sequence Bypass Do not change.	**Off**

SW4

As explained in Chapter 2, it is possible to reduce the Merlin's power consumption by forcing the host side and/or E8860 side of the 89HPES24T6G2 PCIe switch to use 4 lanes instead of 8. In most cases, x4 operation will not affect overall performance and it will reduce power consumption by several watts.

If you are running in a PMC host, then the Host Side PCIe bus is always x4 because the PI7C9X130 PCIe to PCI bridge is a x4, PCIe 1.1 device. But, the E8860 side could still be running x4 or x8. There is absolutely no reason to run it at x8 on a PMC host.

Position	Settings	Default
SW4-1	Off: Merlin Host Side PCIe bus x4 On: Merlin Host Side PCIe bus x8 ***Set to Off when running in a PMC system.***	**Off**
SW4-2	Off: Merlin E8860 PCIe bus x4 On: Merlin E8860 PCIe bus x8 ***Set to Off when running in a PMC system.***	**Off**

SW5

This is a small rectangular pushbutton that is used to restart the STM32F427 on-board control processor and the CX3 MIPI controller.

If you are connected to a Hyperterminal window when you hit reset you will have to exit the program and restart because the USB handshaking in Windows gets confused..

Position	Settings	Default
SW5-1	Press pushbutton to reset STM32F427	**Off**

SW6

This is a small rectangular pushbutton that is used to toggle STM32F427 port bit PA_00. Pressing it will cause the Green, Yellow, and Red LEDs along the edge of the board (side 2) to light up in sequence.

Position	Settings	Default
SW6-1	Press pushbutton to toggle port bit PA_00	**Off**

SW7

SW7-5 controls BOOT0 on the STM.

OFF (BOOT0 = 0) selects firmware programmed into STM flash;

ON (BOOT0 = 1) selects STM bootloader/DFU mode, which uses the STM FS port to access the device holding the image.

(BOOT1 set permanently to "0" with a 1K pulldown to ground)

Position	Settings	Default
SW7-1	Formerly VGA enable. Doesn't work on E8860 Do not change.	**Off**
SW7-2	Off: Normal system power control On: Request STM to reduce core voltage ***Function is not currently implemented.***	**Off**
SW7-3	Off: DisplayPort Ch C on rear connectors On: DisplayPort Ch C on front panel But, see also SW3-1	**On**
SW7-4	Spare, not used.	**Off**
SW7-5	Off:: STM runs from internal flash On: STM boots from external USB device (DFU Mode)	**Off**
SW7-6	Spare, not used.	**Off**
SW7-7	Disable E8860 TESTEN Do not change.	**On**
SW7-8	Standard master clock. Do not change.	**On**

SW8

Select CX3 boot mode to either be:

a) USB (boot directly using USB to obtain boot code from system OS

b) SPI (boot from local flash or if not present, boot from USB)

Settings			Default
SW8-2	**SW8-1**	**Boot Mode**	
On	Off	SPI, On Failure, USB	**selected**
Off	On	Always boot to USB	

5.6.2 MerlinPXC Jumper

JP011D5

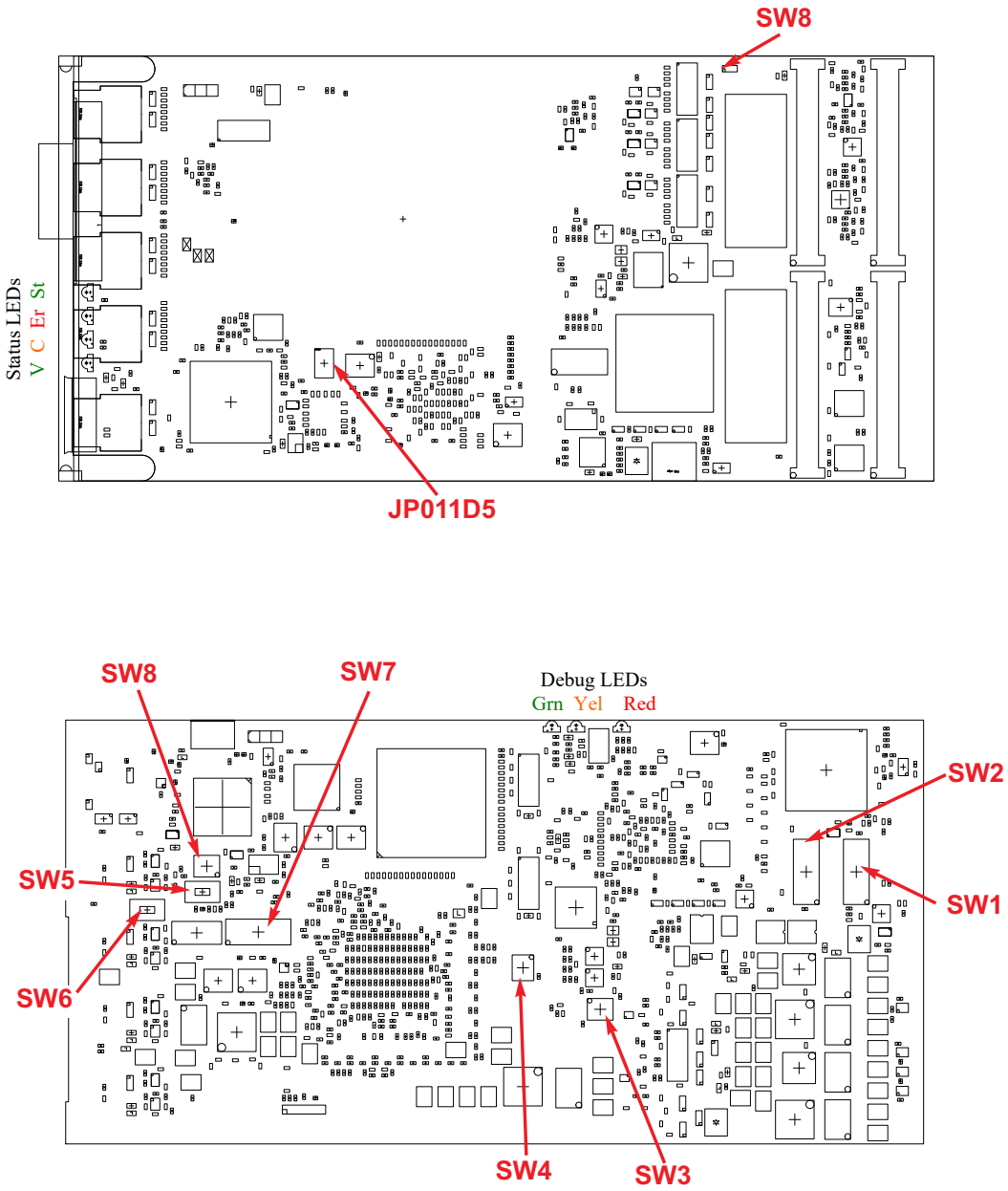
This header is used to select whether the STM OTG_FS port or the OTG_HS port is connected to Mini B USB connector J011D5.

Please see Section 3.9.2 for information about the connector and why you would want to choose one setting over another.

In the table below, the Red and Black refer to the color of the shunts used to make the connections. By convention, HS uses the Black shunts and FS uses Red shunts.

Function	Settings	Default
OTG_HS to J011D5 OTG_FS to uPD720201 Port 1	JP011D5 1-2, 5-6 (Black) JP011D5 3-4, 7-8 (Red)	**No** **No**
OTG_FS to J011D5 OTG_HS to uPD720201 Port 1	JP011D5 1-3, 5-7 (Red) JP011D5 2-4, 6-8 (Black)	**Yes** **Yes**

Figure 5-3 MerlinPXC Switch Packs and Jumpers Locations



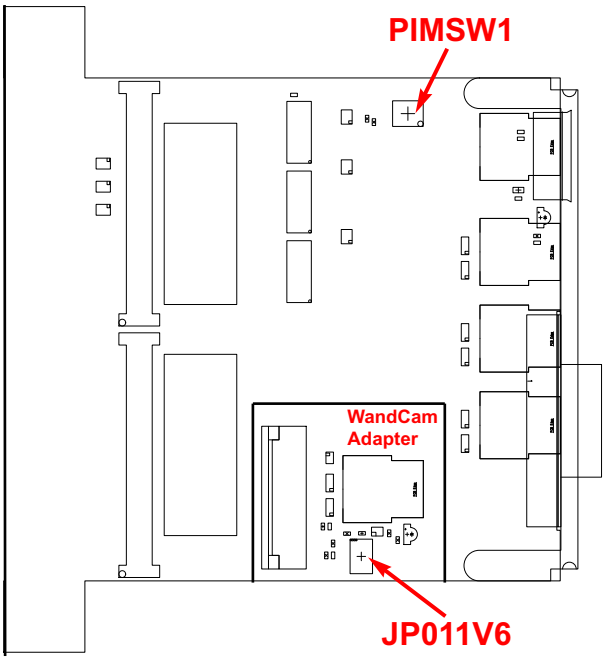
5.6.3 MerlinPXC PIM Switch Pack

PIMSW1

Select alternate configurations for PIM

Position	Settings	Default
PIMSW1-1	Off: select PMC Pn4 as source for DisplayPort channels On: select XMC Pn6 as source for DisplayPort channels See Section 3.17 for more information	**Off**
PIMSW1-2	Off: disable DP Ch C and F and pass VGA onto PIM On: normal operation, DP C, D, F all work	**On**

Figure 5-4 MerlinPXC PIM Jumper Locations



5.6.4 MerlinPXC PIM WandCam Header

JP011V6

These jumpers are used to control pins on the WandCam paddleboard.

Function			Settings		Default
PDW_XCLK_R	24MHz Clock Source	JP011T4	1-2	Red	yes
PDW_XCLK_J	Clock input to camera				
PDW_PDN	Tied to pulldown to prevent camera from going into power down. Do not use – testing only				
PDW_XRST_L	10K/0.1uf RC to make a simple reset	JP011T4	3-5	Black	no
PDW_XRST_J	Reset input to camera				
PDW_XRST	Possible reset source form host. If it exists, use instead of PDW_XRST_L	JP011T4	5-6	Red	no
-	Not used	JP011T4	7, 8	-	-

5.7 MerlinMTX Switch Packs and Jumpers

The MerlinMTX has 4 switch packs and 2 jumper positions. Where practical, switch packs were used because they are easier to use.

5.7.1 MerlinMTX Switch Packs

As explained in Chapter 2, it is possible to reduce the Merlin's power consumption by forcing the host side and/or E8860 side of the 89HPES24T6G2 PCIe switch to use 4 lanes instead of 8. In most cases, x4 operation will not affect overall performance and it will reduce power consumption by several watts.

SW1-1 and SW1-2, respectively, control the lane width for the E8860 and host ports of the 24T6.

SW1

Position	Settings	Default
SW1-1	Off: Merlin E8860 PCIe bus x4 On: Merlin E8860 PCIe bus x8	**Off**
SW1-2	Off: Merlin Host Side PCIe bus x4 On: Merlin Host Side PCIe bus x8	**Off**
SW1-3	Spare, not used.	**Off**
SW1-4 SW1-5	JTAG Loop Bypass Do not change.	**SW1-4 Off** **SW1-5 On**
SW1-6	Enable Host JTAGRST Do not change.	
SW1-7	Off: VPWR = 5V On: VPWR = 12V	**Off**
SW1-8	Power Sequence Bypass Do not change.	**Off**

SW2

This is a small rectangular pushbutton that is used to restart the STM32F427 on-board control processor.

If you are connected to a Hyperterminal window when you hit reset you will have to exit the program and restart because the USB handshaking in Windows gets confused..

Position	Settings	Default
SW2-1	Press pushbutton to reset STM32F427	**Off**

SW3

This is a small rectangular pushbutton that is used to toggle STM32F427 port bit PA_00. Pressing it will cause the Green, Yellow, and Red LEDs along the edge of the board (side 2) to light up in sequence.

Position	Settings	Default
SW6-1	Press pushbutton to toggle port bit PA_00	**Off**

SW4

SW4-5 controls BOOT0 on the STM.
(BOOT1 set permanently to "0" with a 1K pulldown to ground)

OFF (BOOT0 = 0) selects firmware programmed into STM flash;

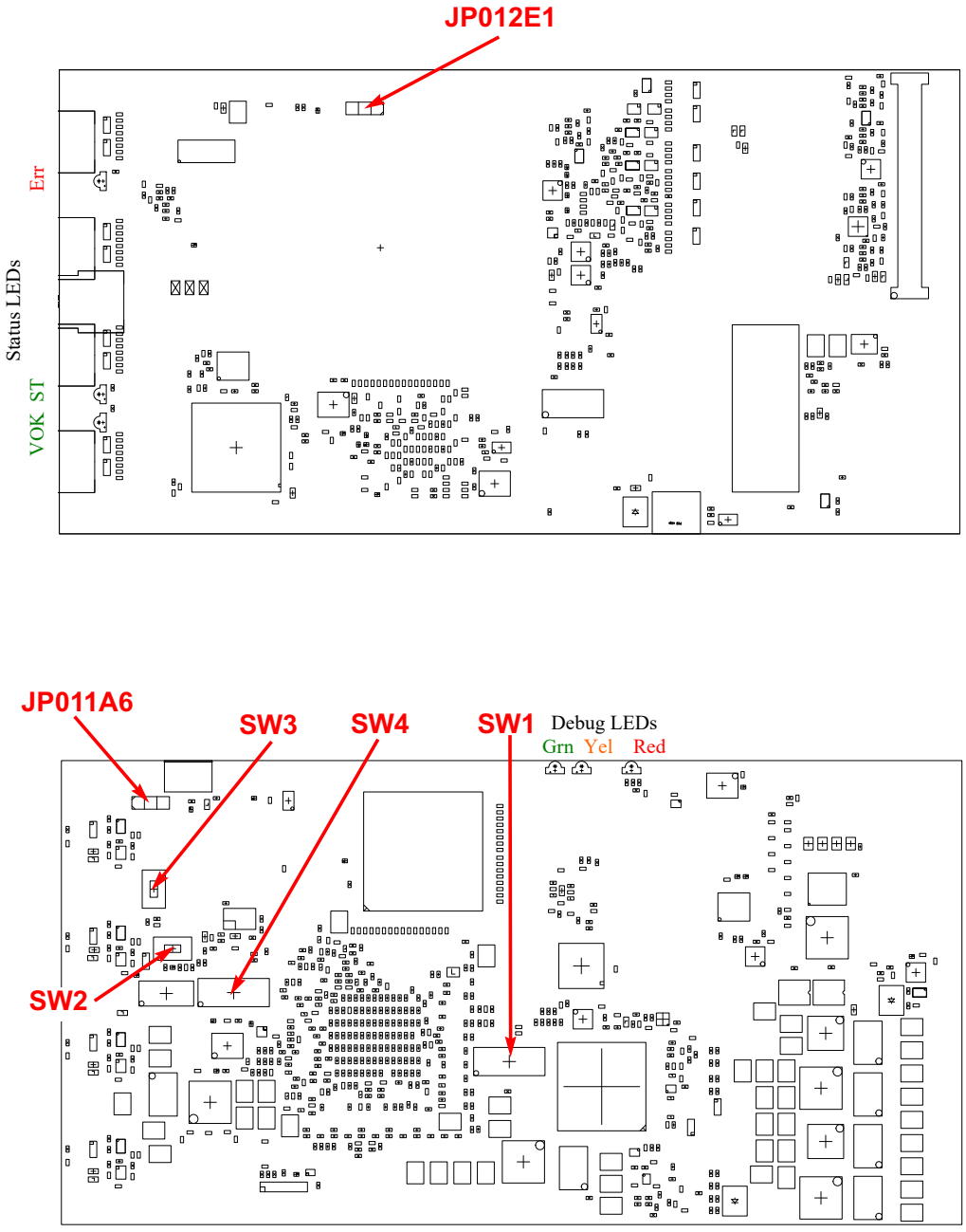
ON (BOOT0 = 1) selects STM bootloader/DFU mode, which uses the STM FS port to access the device holding the image.

Position	Settings	Default
SW4-1	Formerly VGA enable. Doesn't work on E8860 Do not change.	**Off**
SW4-2	Off: Normal system power control On: Request STM to reduce core voltage ***Function is not currently implemented.***	**Off**
SW4-3	Off: DP/DVI Ch C on rear connectors Do not change. On: DP/DVI Ch C on front panel	**Off**
SW4-4	Spare, not used.	**Off**
SW4-5	Off: STM runs from internal flash On: STM boots from external USB device (DFU mode)	**Off**
SW4-6	Reserved. Do not change.	**Off**
SW4-7	Disable E8860 TESTEN Do not change.	**On**
SW4-8	Standard master clock. Do not change.	**On**

5.7.2 MerlinMTX Jumpers

JP012E1 and JP011A6 are reserved for debugging and testing.

Figure 5-5 MerlinMTX Switch Packs and Jumpers Locations



5.7.3 MerlinMTX PIM Switch and Jumpers

There are no user switches or jumpers on the MerlinMTX PIM.

5.8 Agate or Merlin Installation Notes

When first trying out the Agate or Merlin, if possible, try using it in a known good working system that has already had a graphics board installed in the same location that you are putting the Rastergraf board.

Why? It's best to change as few things as possible since most systems are totally dependent on a functioning graphics display.

The Agate or Merlin can plug into any

a) 32 or 64-bit, 33 – 133 MHz, PCI/PCI-X compatible, 3.3 or 5V signaling, IEEE 1386-2001 compatible single module PMC location, or

b) x1, x4 or x8 lane PCIe 1.1 or PCIe 2.0 compatible, VPRW=5V or 12V (VPWR=5V is strongly advised), VITA 42.3 XMC location, or

c) a location that supports both PMC and XMC. In such a case, the board will automatically choose to run as a PCIe device.

If you plan to use the video input functions on PMC, it must be at least 66MHz and 64-bit, 66MHz is much better. If at all possible, use an XMC position instead if you are going to do video input.

Please also review Section 5.2 before continuing.

Assuming that there are no limitations on bus speed or power supplies, the Agate or Merlin should be able to operate in most any VME, VPX, CompactPCI, or CompactPCI Serial computer. The boards will also work in CompactPCI or PCI systems by using a carrier.

Important Compatibility Note:

While the graphics boards will work in a PCI or CompactPCI passive (no on-board bridge) carriers, for best reliability it is recommended that you use an active (on-board bridge) PCI or CompactPCI carrier.

The following sections cover installation in a variety of systems:

Section 5.9 Installing the Board on a CPU

Section 5.10 Installing the Board on a Carrier

Note:

We want you to succeed. Please know that if you are willing to loan Rastergraf your system, Rastergraf will verify its operation with the Agate or Merlin at no charge unless there are serious difficulties.

5.9 Installing on a CPU

You can install an Agate or Merlin board in a wide variety of systems, either mounting it directly on a CPU board or on a carrier (or adapter) that has a PMC and/or XMC location on it and a bus interface to the host system.

Systems that support direct CPU or carrier-based installations include:

VMEbus

CompactPCI

CompactPCI Serial

ATCA

OpenVPX

Systems that have available PMC and/or XMC carriers include:

PCI

PCIe

Please see Section 5.8 for the carrier-based installation.

Some basic installation ground rules.

For PMC Installations:

a) The system MUST be able to supply:
3.3V@2A (peak, 1s) and
5V@7A (peak, 1s);

b) The graphics board features a "Universal PMC/PCI" interface and can operate in a PMC location that uses either 5V or 3.3V signaling.

For XMC Installations:

a) The system MUST be able to supply:
3.3V@2A (peak, 1s) and
VPWR = 5V@7A (peak, 1s) or VPWR = 12V@3.3A (peak, 1s);

b) Rastergraf ***always*** recommends that when there is a choice, ***set VPWR to 5V*** (not 12V);

c) The host XMC connectors must provide x4 or x8 PCIe lanes..
x1 is OK but just for modest performance graphics-only applications.

1. Review the settings for your graphics board. Refer to Section 5.4 for Agate settings or Section 5.5 for Merlin settings;
2. Shut down the operating system and turn off the power;

Warning!

Never open the computer without turning off the power supply. You can easily get shocked, ruin computer parts or both unless you turn off the power. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. Even with power switched off, lethal voltages can exist in the equipment.

Caution

Be careful not to remove the board from its antistatic bag until you are ready to install it. You should always were a grounded wrist strap whenever handling any computer boards.

3. Open the computer;
4. Remove the CPU board onto which the graphics board is to be installed and locate an empty PMC, XMC, PMC/XMC site. If you install in a PMC/XMC site, the graphics card will use the XMC (PCIe) bus interface;
5. Touch a metal part of the computer chassis, remove the graphics board from its anti-static bag, and mount the board evenly and carefully onto the connectors. Refer to the illustrations on the following pages.

Note

Sometimes the graphics board front panel can hang up going into the front panel opening. This can be because there is an EMI gasket that is installed in a slot cut into the graphics board front panel. If the hole in the carrier board is “on the small side” it can make it difficult to install the graphics board. In this case, you will have to remove and discard the gasket.

6. After ensuring that the board is seated correctly, install the mounting screws (two near the front and two near the PMC and XMC connectors);
7. Close the computer.

Now, please go to Section 5.11 for Connecting to Rear I/O or Section 5.12 for Connection to the Front Panel.

Figure 5-6 Installation onto an Emerson MVME2604

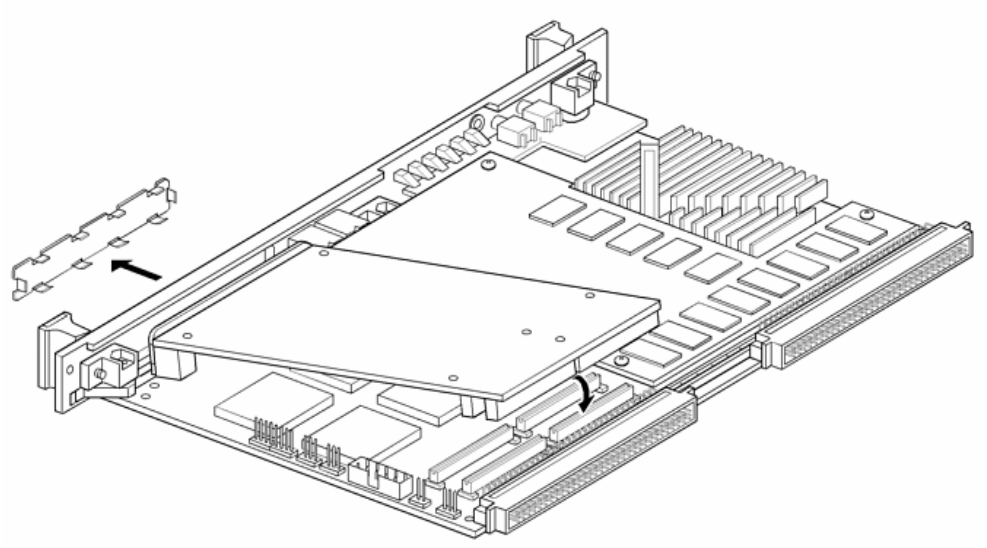


Figure 5-7 Installation onto an Emerson CPV3060

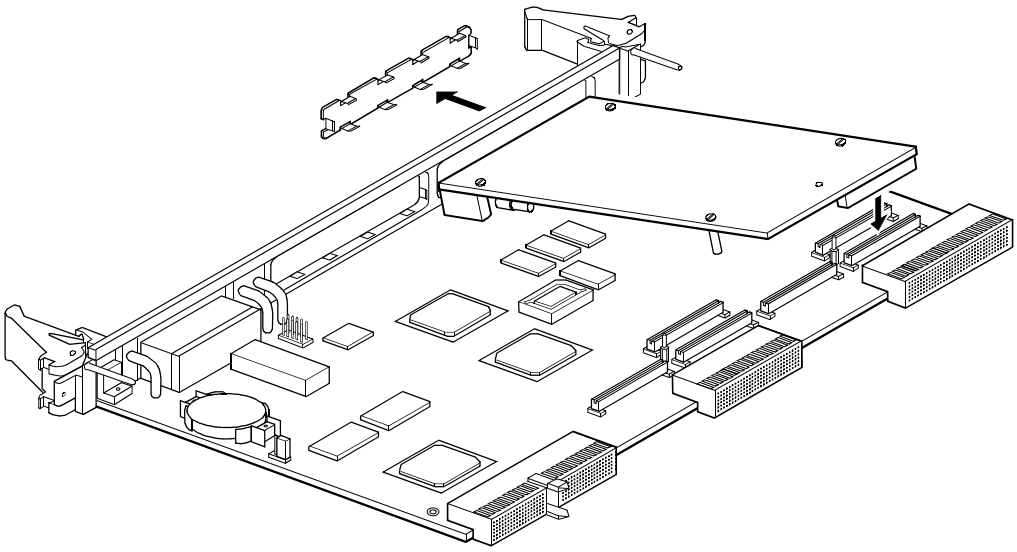


Figure 5-8 Installation onto a CW Defense VPX6-1952

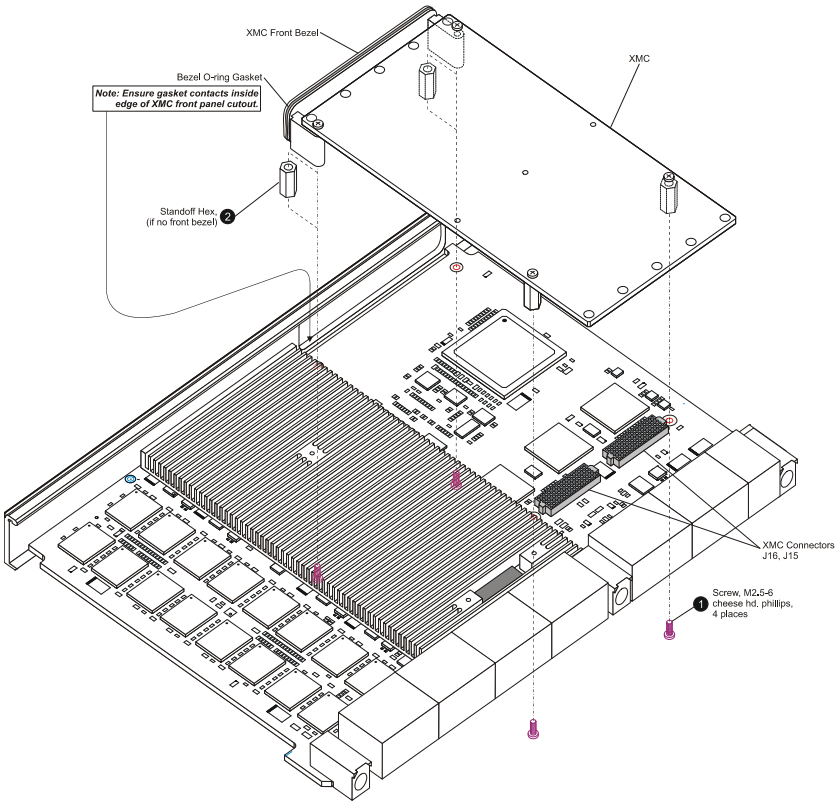
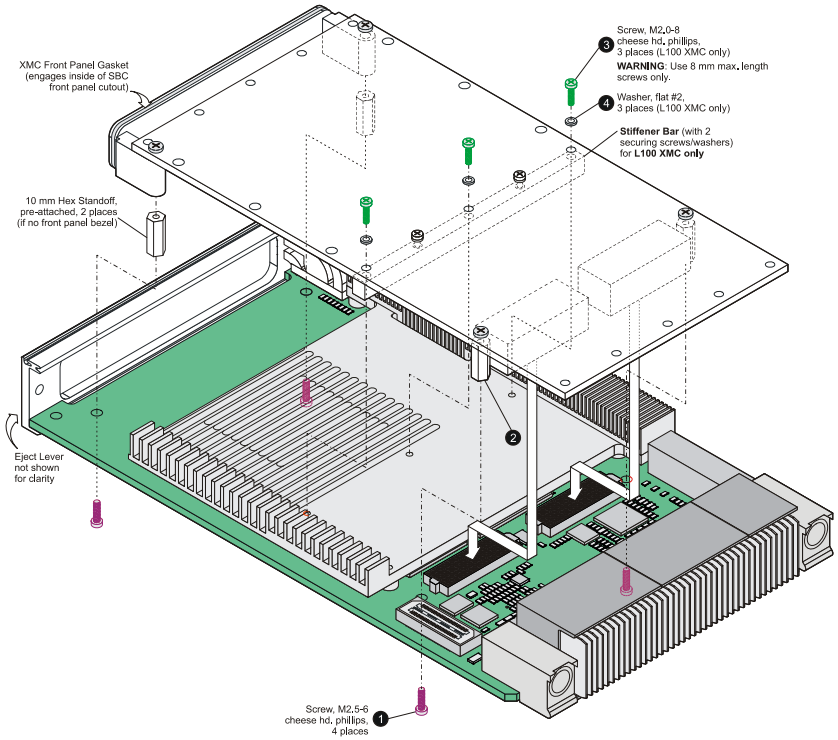


Figure 5-9 Installation onto a CW Defense VPX3-1252



5.10 Installing the Graphics Board on a Carrier

This section covers installing your board on a carrier that is then itself installed in the host system. The procedure is similar to the host-based method outlines in Section 5.7, but there are enough differences to warrant a separate section. However, the same provisos apply:

For PMC Carrier Installations:

a) The carrier MUST be able to supply:
3.3V@2A (peak, 1s) and
5V@7A (peak, 1s);

b) The graphics boards feature a "Universal PMC/PCI" interface and can operate in a PMC location that uses either 5V or 3.3V signaling.

For XMC Carrier Installations:

a) The carrier MUST be able to supply:
3.3V@2A (peak, 1s) and
VPWR = 5V@7A (peak, 1s) or VPWR = 12V@3.3A (peak, 1s);

b) Rastergraf ***always*** recommends that when there is a choice, ***set VPWR to 5V*** (not 12V);

c) The XMC connectors must provide x4 or x8 (not x1) PCIe lanes.

Caution

Be careful not to remove the board from its antistatic bag until you are ready to install it. You should always were a grounded wrist strap whenever handling any computer boards.

1. Review the settings for your graphics board. Refer to Section 5.4 for Agate settings or Section 5.5 for Merlin settings;
2. Review the settings for your carrier board;
3. Locate an empty PMC, XMC, PMC/XMC site on your carrier board (sometimes there are 2 sites) and install the graphics board on the carrier, carefully and evenly settling it onto the PMC and/or XMC connectors. If you install in a PMC/XMC site, the graphics card will use the XMC (PCIe) bus interface;

Note

Sometimes the graphics board front panel can hang up going into the front panel opening. This can be because there is an EMI gasket that is installed in a slot cut into the graphics board front panel. If the hole in the carrier board is “on the small side” it can make it difficult to install the graphics board. In this case, you will have to remove and discard the gasket.

4. Make sure to secure the graphics board to the carrier using the standoffs and screws provided;
5. Shut down the operating system and turn off the power;

Warning!

Never open the computer without turning off the power supply. You can easily get shocked, ruin computer parts or both unless you turn off the power. Unless internal AC wiring is exposed, leave the power cord plugged in, so as to ground the computer chassis. Even with power switched off, lethal voltages can exist in the equipment.

6. Open the computer;
7. For a non-motherboard installation, find the empty slot in the card cage that is closest to the CPU. If possible, try to optimize airflow by blocking off unused slots in the card cage;

   For a motherboard installation, check its User Manual to locate a PCIe slot that supports at least x4 lanes, preferably PCIe 2.0 or a PCI slot that supports at least 32-bit, 66 MHz.

i. Touch a metal part of the computer chassis and mount the graphics board/carrier board assembly evenly and carefully onto the connectors. Refer to the illustrations on the following pages..

8. If possible, try to optimize airflow so that the graphics board gets a good airflow. This is especially hard to attain in a PCI or PCIe system and the failure to do so will result in an overheated graphics board. If nothing else, get an extra CPU fan and secure it so that it is blowing right on the exposed side of the graphics board.
9. After ensuring that the carrier board is seated correctly, install the relevant mounting screws;
10. Close the computer.

Now, please go to Section 5.11 for Connecting to Rear I/O or Section 5.12 for Connection to the Front Panel.

Figure 5-10 Installation onto a PCI Carrier

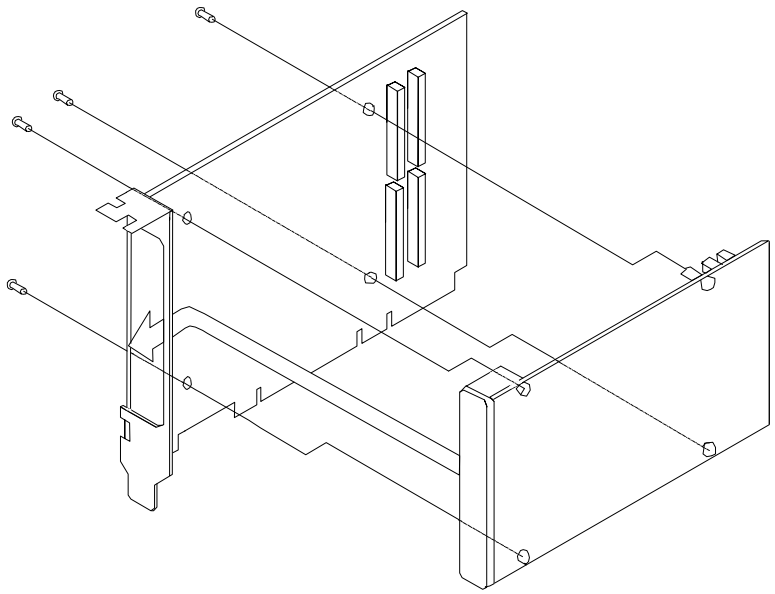


Figure 5-11 Installation of a PCI Module into an Emerson MTX

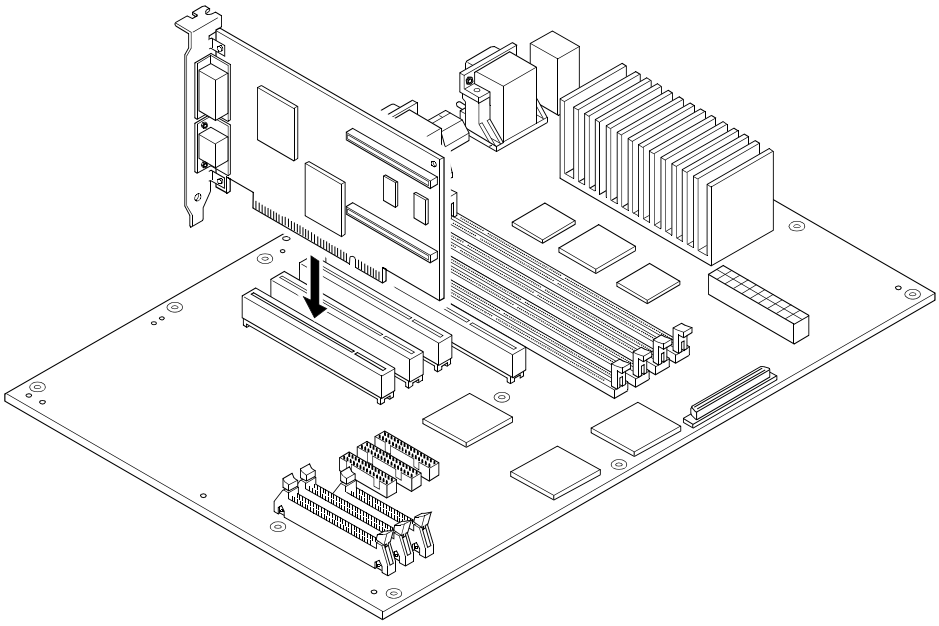


Figure 5-12 Installation onto a 3U CPCI Carrier

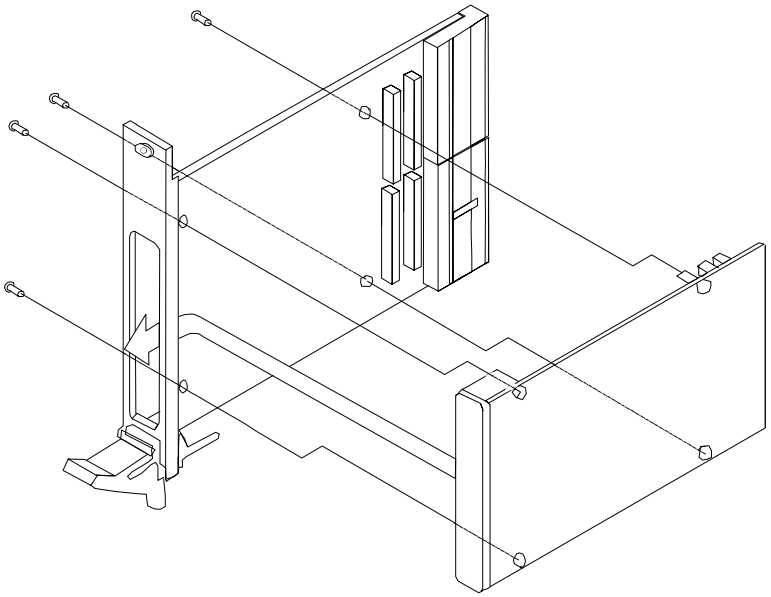


Figure 5-13 Installation onto a 6U CPCI Carrier

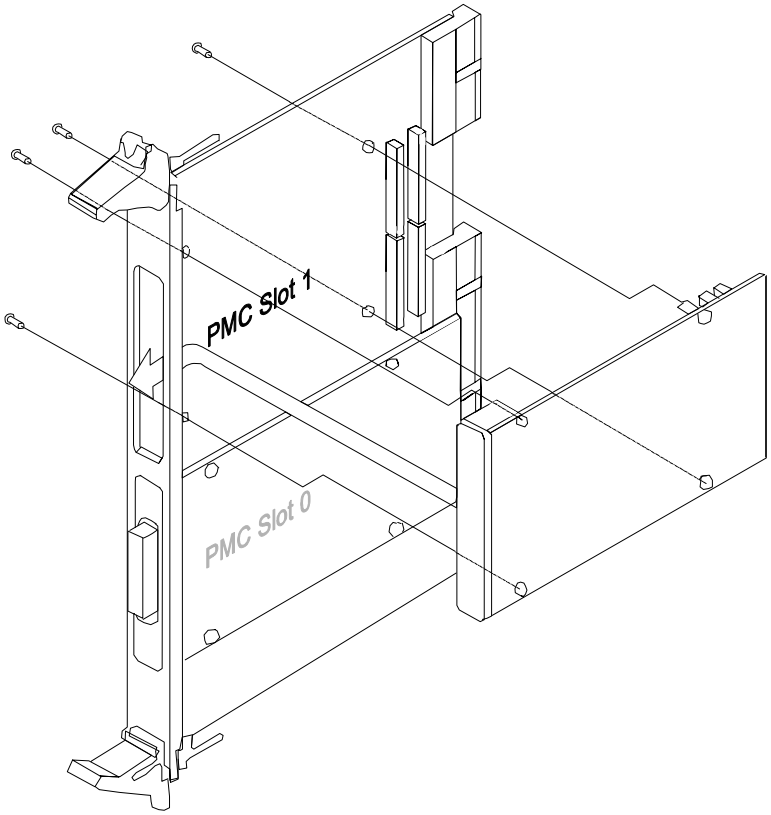
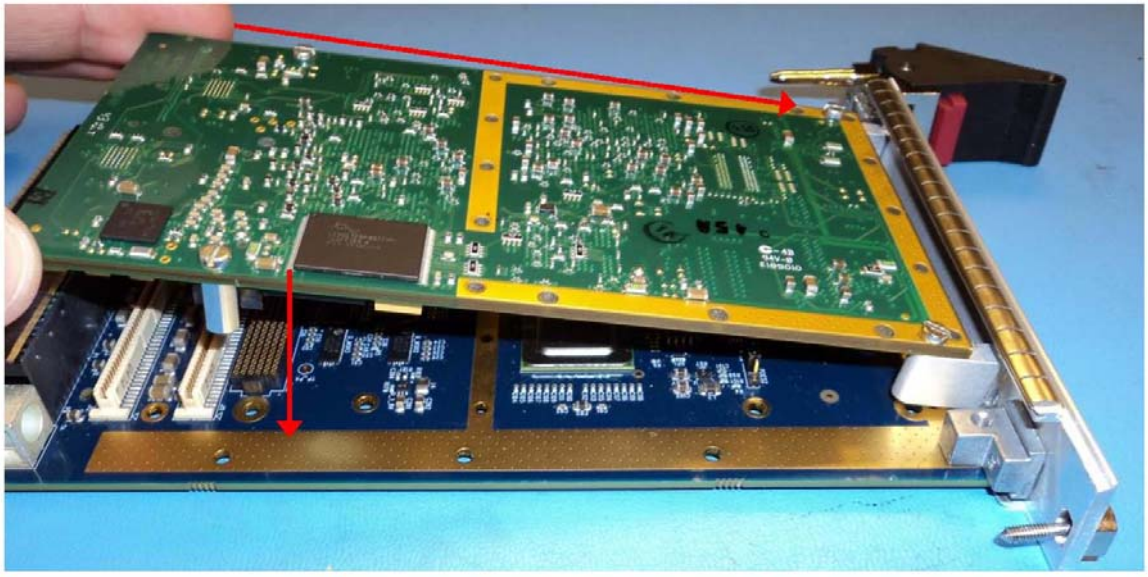


Figure 5-14 Installation onto a 3U Acromag VPX4810 OpenVPX Carrier



5.11 Rear I/O Connections

Connecting to the Rear I/O can be a major project in and of itself. Chapter 4 is dedicated to providing as much reference information as possible to ease this task, but in many cases you will be on your own and it is beyond the scope of this manual to do more than has been done in Chapter 4.

As already mentioned elsewhere in this manual, Rastergraf has designed PIM (PCI Interface Module) connector boards in the hope of easing the rear access integration, The PIM mounts on a third-party-supply RTM (Rear Transition Module) that is purpose-built to support PIMs. Please see Section 4.3 for much more information about PIMs.

Because rear access applications are so varied and the card cages, enclosures, and frames are of all sorts, this manual does not attempt to advise an installation procedure for the RTM and PIM. It is, as it is said, left as an exercise for the reader.

That said, here are some suggested steps that should be taken:

a) determine if your CPU vendor can supply an RTM that has a PIM location on it. If so, then using the appropriate Rastergraf PIM would be the quickest way to getting pictures.

b) if your CPU vendor cannot supply an RTM, or not one with a PIM site, then you will need to research the available RTMs for your bus. See Section 4.2 for more information.

   Part and parcel to this will be to verify that the pinout of the RTM matches the CPU board.

   Full support for PMC Pn4 seems to be much more prevalent than XMC, so if you can use the Agate or Merlin Pn4 I/O you will have better luck. Again, see Chapter 4 where all of this is covered in great detail.

c) if neither (a) nor (b) is going to work, then it seems like all that is left for you will be to build your own RTM, if you have a custom installation that can justify that process, or you will have to build cables and attach them to the backplane (also covered in Chapter 4). Needless to say, this is the least desirable of all solutions.

Now, please skip to Section 5.13

5.12 Front Panel Connections

There isn't a lot to say about making the front panel connections.

In the case of both VGA and DisplayPort, the OS will figure out what channels are plugged in and choose a console screen appropriately. In general, it's best to select the lowest order connector first, if you are only using one monitor.

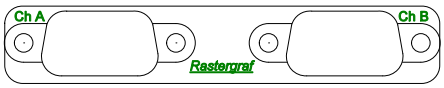
After you have the graphics chip software installed, you will have flexibility to configure the display format, and in the case of multiple screens, determine the order of the screens on your desk.

A note about connector security: while the VGA, Agate Multi-Function I/O, and LVDS connectors all have very secure thumbscrew attachments, the Mini DisplayPort and USB connectors rely on latches to retain the cables. As long as the connector is fully inserted in the connector, this works pretty well, but it won't ever be as secure as thumbscrews. So, if this is an issue, you will need to devise an external retention (like a tie-wrap to something) to help retain the cable.

Figure 5-15 AgatePXC and Merlin PXC Model Front Panel Identifier

AgatePXC/2: 2x MiniDisplayPort + I/O

AgatePXC/1V: 2x VGA

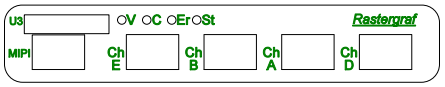


AgatePXC/1D: 2x MiniDisplayPort

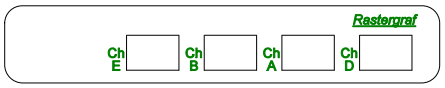
AgatePXC/1L: 1x LVDS

AgatePXC/1R: 1x VGA

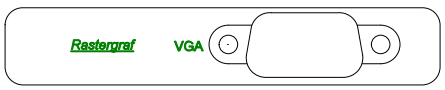
MerlinPXC/2: 4x MiniDisplayPort + I/O



AgatePXC/1D: 2x VGA



MerlinPXC/1V: 1x VGA



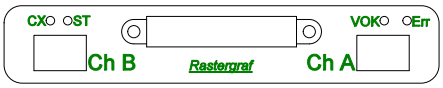
The MerlinMTX has no front panel connectors

5.13 Initial Checks

A good first check, once verifying that everything is securely plugged in, is to turn on the computer and check the LEDs on the Rastergraf board.

5.13.1 AgatePXC/2 and PIM LEDs

On the AgatePXC/2 there are four LEDs on the front panel:



CX	yellow LED	should be blinking off and on at boot up. If you load an application program into the CX3, the LED will no longer be active. Pressing SW5 will reset the CX3 and make it go back to blinking.
ST	green LED	should ALWAYS be slowly blinking off and on. If it isn't, something is wrong with the board or installation that has made the auto-startup ST ISM program crash. Pressing SW5 will reset the ST ISM and make it go back to slowly blinking.
VOK	yellow LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.
Err	red LED	should ALWAYS be OFF. If it is ON, the board is in an error state, most likely overheating. Turn the computer off and investigate.

On the AgatePXC/2 Side 2 (the side of the board you can see when the board is plugged in), are 3 LEDs (see Figure 5-1).

If you press SW6, it will cause the Green, Yellow, and Red LEDs to light up in sequence.

Also on Side 2, on the edge opposite the Green, Yellow, and Red LEDs, is the FX3 status. It functions the same way as the CX LED (see above) and is also reset by pressing SW5.

On the AgatePXC/2 PIM, you see exactly the same front panel as the front of the AgatePXC/2 itself but most of the LEDs are not valid:

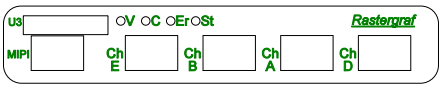
CX	Not installed	
ST	Not installed	
VOK	green LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.
Err	Not installed	

On the AgatePXC/2 WandCam Adapter boardlet there is one LED

VOK	green LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.

5.13.2 MerlinPXC/2 and PIM LEDs

On the MerlinPXC/2 front panel there are four LEDs:

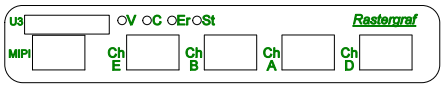


V	yellow LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.
C	yellow LED	should be blinking off and on at boot up. If you load an application program into the CX3, the LED will no longer be active. Pressing SW5 will reset the CX3 and make it go back to blinking.
Err	red LED	should ALWAYS be OFF. If it is ON, the board is in an error state, most likely overheating. Turn the computer off and investigate.
St	green LED	should ALWAYS be slowly blinking off and on. If it isn't, something is wrong with the board or installation that has made the auto-startup ST ISM program crash. Pressing SW5 will reset the ST ISM and make it go back to slowly blinking.

On the MerlinPXC/2 Side 2 (the side of the board you can see when the board is plugged in), are 3 LEDs (see Figure 5-3).

If you press SW6, it will cause the Green, Yellow, and Red LEDs to light up in sequence.

On the MerlinPXC/2 PIM, you see exactly the same front panel as the front of the AgatePXC/2 itself but most of the LEDs are not valid:



V	green LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.
C	Not installed	
Er	Not installed	
ST	Not installed	

On the MerlinPXC/2 WandCam Adapter boardlet there is one LED

VOK	green LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.

On the MerlinPXC/2 PIM VGA Adapter boardlet there is one LED

VOK	green LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.

5.13.3 MerlinMTX and PIM LEDs

On the MerlinMTX Side 1 where there would be a front panel if there were on, are three LEDs on the front panel (see Figure 5-5).

You may not be able to see the LEDs because of the front panel hardware, which isn't very convenient. Yes, the LEDs should really be on Side 2.

V	yellow LED	should ALWAYS be on. If it isn't, something is wrong with the board or the installation.
Err	red LED	should ALWAYS be OFF. If it is ON, the board is in an error state, most likely overheating. Turn the computer off and investigate.
St	green LED	should ALWAYS be slowly blinking off and on. If it isn't, something is wrong with the board or installation that has made the auto-startup ST ISM program crash. Pressing SW2 will reset the ST ISM and make it go back to slowly blinking.

On the MerlinMTX/2 Side 2 (the side of the board you can see when the board is plugged in), are 3 LEDs (see Figure 5-5).

If you press SW3, it will cause the Green, Yellow, and Red LEDs to light up in sequence.

5.14 Finishing the Installation

Please see Chapter 8, Sections 8.10-8.12 for suggested software installations procedures for Windows and Linux.

> **Note:**
>
> We want you to succeed. Please know that if you are willing to loan Rastergraf your target display, Rastergraf will verify its operation at no charge unless there are serious difficulties.

5.14.1 Connecting to your Display

The best thing when you first start is to keep it simple. When first trying out the Agate or Merlin, if possible, try using in a known good working system that has already had a graphics board installed in the same location that you are putting the Rastergraf board.

Why? It's always best to change as few things as possible, especially when it is unfamiliar hardware and software. Also, for the display, don't start off by using DP dongle. Locate a standard VGA or DisplayPort monitor (many do both) and start with that.

So, in the case of VGA, it's easy, just plug into a standard "multi-sync" VESA compatible monitor and you should get an image. Don't try to do anything special like composite sync on green or 4-wire RGBS. Just go with a standard off-the-shelf VGA cable that supports DDC.

In the case of DisplayPort, likewise, having plugged a Mini DisplayPort-to-DisplayPort adapter cable between the Agate or Merlin and your monitor, you should get a picture right off.

If you are starting with LVDS, none of this will help. In this case, try to ensure that the LVDS setup is KNOWN to work with some other system so you are not trying to troubleshoot 2 things at once.

5.14.2 Checking your Display

If you have a PC, the BIOS firmware in the graphics board will be invoked and you should get some sort of display on power-up.

But, if you have a PowerPC system running VxWorks, for example, in virtually all cases, you will not get any visual indication that the board is operational until run some graphics board-specific. If you have such a system and are ever in doubt about whether the board really works, you would be well advised to plug it into a PMC to PCI carrier and plug it into a PC to try it out.

5.15 Using a Rastergraf Board in a PC

You will certainly have to install some software to fully utilize the Agate or Merlin because the OS will probably not know about the CX25858 digitizer, the CX3 and FX3 controllers, and, in the case of XP and W7, the uPD720201 USB host controller. Since they are USB-based devices, the OS won't even see the CX3 or FX3 until the USB drivers are installed.

Note:

As of this date, the full software suite has been tested on XP, Window 7, (W7), and Windows 10 (W10). Of all of these, W7-64 Pro is the version we recommend for Agate. W10-64 Pro is fine for Merlin.

The Agate display driver is not supported by AMD beyond W7, and does not, in fact work on W10. The OS degrades to the dumb frame buffer Microsoft Basic Display Driver which gives you one screen at 1600x1200 max. Also, the video capture rate is degraded because of the slow graphics operation.

In the case of Linux, please also contact Rastergraf as to whether we have tested on your particular version. Agate development has been frozen by AMD, so any AMD-sourced driver may not be satisfactory. X.org has a separate code stream and may work better on later OS versions.

In summary, software will be needed for:

Device	Description	Agate or Merlin	Software Source
89HPES24T6G2	PCIe-PCIe Switch	All	OS Auto-install
PI7C19130	PCI-PCI Bridge	Agate, MerlinPXC	OS Auto-install
E4690	Graphics Controller	Agate	AMD, Rastergraf
E8860	Graphics Controller	Merlin	AMD, Rastergraf
uPD720201	USB Host Controller	Agate, MerlinPXC	Auto or Rastergraf
CX3	MIPI Controller	Agate, MerlinPXC	Cypress, Rastergraf
FX3	USB Controller	Agate	Cypress, Rastergraf
CX25858	A/V Digitizer	Agate, MerlinMTX	Rastergraf
ADV7441A	RGBHV/DVI Digitizer	Agate	Rastergraf
STM32F427	System Monitor CPU	All	ST Micro, Rastergraf
PLDs	On-board Controls	All	Rastergraf
LM63, LM75	Temperature Sensors	All	Rastergraf

You can download the necessary drivers from the Rastergraf web site. Please contact us for an ftp link.

5.15.1 Single Graphics Board

If you are using a PC and the Rastergraf board is to be the system display (and you don't have another VGA controller installed), the system BIOS should find the Rastergraf board, and initialize the display.

5.15.2 Multiboard Operation

If you have another Rastergraf graphics board in the system, the order in which the boards are plugged into the backplane or motherboard will determine which board will be used for the system display. If the BIOS picks the wrong one, turn off the computer and swap the boards' positions.

If your system has a non-removable VGA controller and you want to use the Rastergraf board as the system display you should be able to disable it with a BIOS setting or set the BIOS to prefer PCIe or PCI over the internal graphics.

If the computer still boots the internal graphics, there may be something wrong with the Rastergraf board installation.

5.16 Using a Rastergraf Board in a PowerPC

You will have to boot using a serial terminal and only after the graphics software has been installed and run will you see anything.

5.17 Final Checks

If you are running in a PC, then you should get the usual PC displays. If you have multiple graphics boards installed, only one will be initialized by the BIOS. Once you have installed the Windows XP/7 multihead drivers and reboot, all screens will be initialized as the OS boots.

In the case of X Windows, your monitor should display a uniform stippled raster and a cross-hair cursor, which is controlled by the mouse. If you have multiple graphics boards installed, all screens will be initialized and display the stipple once you have the server installed and running.

For SDL, demo programs are provided that may be run to put test patterns on the screen(s).

Pictures!

Once you have a picture on the screen, you may need to adjust the width, height, brightness, contrast, and hold controls on your monitor to get a good, centered image. If these controls don’t adjust the image properly, the parameters used to set the graphics timing registers might be wrong. If

you have any trouble with any part of the installation call or email Rastergraf for assistance, or refer to Chapter 7.

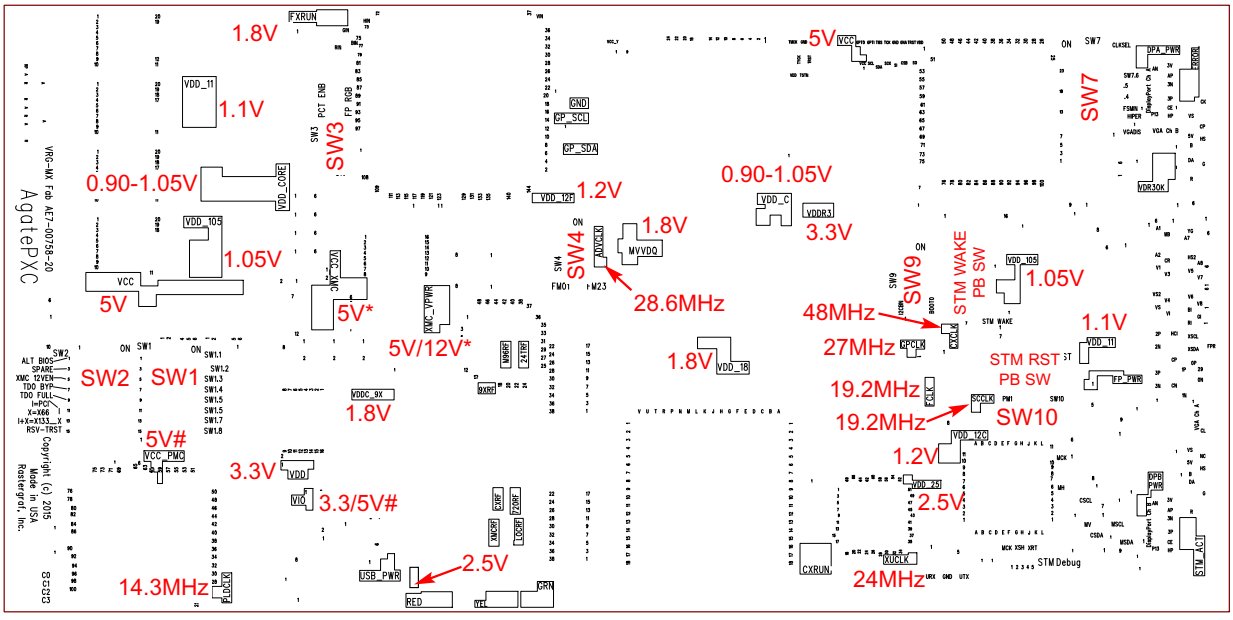
5.18 Test Points

There are a variety of voltage and frequency test points on the side of the board exposed when it is plugged into a host board.

Needless to say, poking around the board is to be done at your risk, and if you damage the board it might be fixable. In any case, take very good care if you do this.

The following figures detail the accessible points.

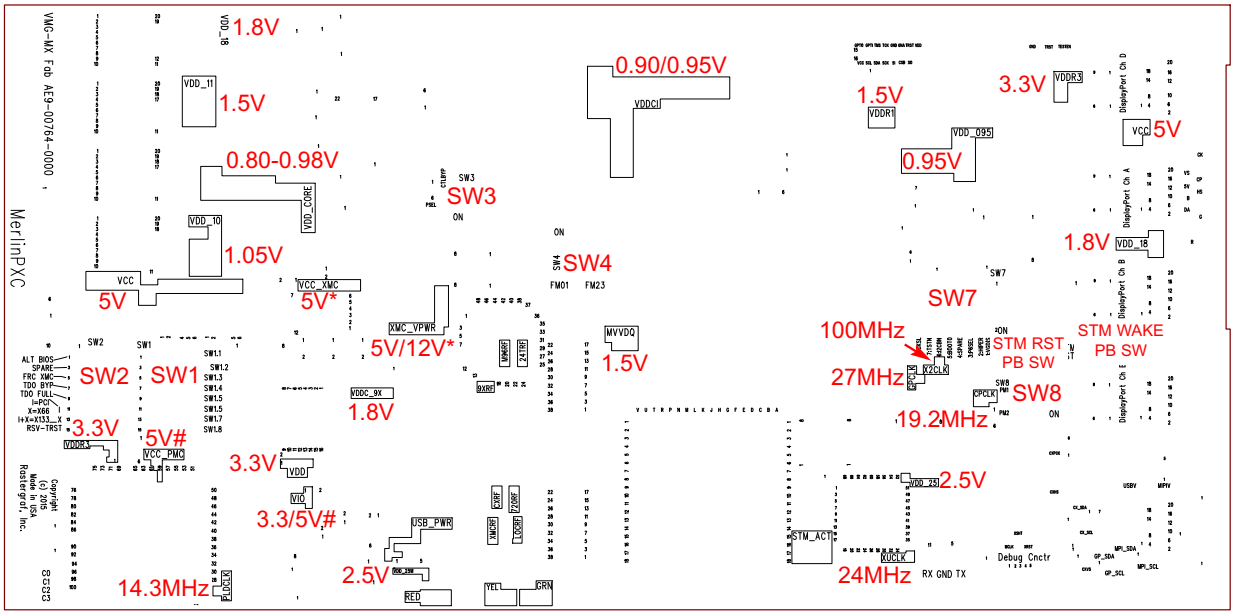
Figure 5-16 AgatePXC Test Points



Valid when plugged into a PMC site

* Valid when plugged into an XMC site

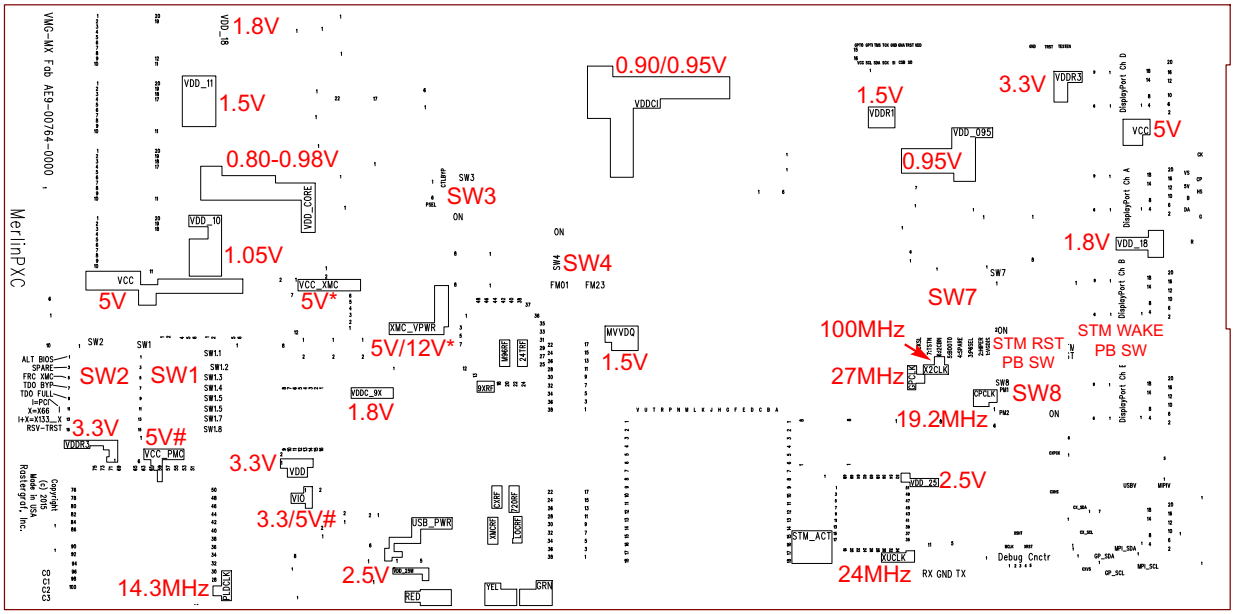
Figure 5-17 MerlinPXC Test Points



\# Valid when plugged into a PMC site

* Valid when plugged into an XMC site

Figure 5-18 MerlinMTX Test Points



\# Valid when plugged into a PMC site

* Valid when plugged into an XMC site

Chapter 6
Programming On-board Devices and Memories

6.1 Introduction

The graphics boards are mostly an assemblage of “black box” parts and there isn’t a lot of external logic that goes between them. It would be best to review the Functional Description in Chapter 1 as it will suffice for all major elements in both designs. In depth information can be gotten by going to vendors’ web sites directly and obtaining data sheets..

Unfortunately, the data sheets for the CX25858 digitizer and the AMD graphics chips data sheets only available under NDA. If you need access to any of these, please contact Rastergraf and we will try to help you.

The following sections cover only the specialized devices that form the underlying glue for the designs. They are intended to supply information unique to the use of that particular chip on the Agate or Merlin.

As mentioned elsewhere, Rastergraf offers a variety of software to support these graphics boards running under Windows XP, 7, etc., VxWorks, and Linux. These offerings are covered in detail on the Rastergraf web page (http://www.rastergraf.com/) or contact Rastergraf with your specific requirements.

This chapter includes the following other sections:

6.2 PLDs and the Auxiliary Control Registers

The Agate and Merlin both use Lattice LC4ZE series PLDs to implement a variety of functions including status and control bits, power sequencing, and "glue-logic" substitution. The PLDs are linked to the STM32F427 Integrated System Monitor via the GP I^2C bus. In addition to the STM, programmed I/O bits on the 24T6 switch can be used by the host OS to simulate I^2C, thus giving the host the ability to access the PLD CSRs.

The PLDs depend not only on system 3.3V but also 1.8V, which is a local DC-DC switcher-generated power source. In order to avoid power startup problems, some of the PLDs use a linear regulator that is independent of the switcher subsystem to provide 1.8V directly from 3.3V.

In the cases where a PLD are not included, the functions are either not needed or are supported instead by the ST ISM firmware.

There are 3 PLDs:

a192000p (Agate, MerlinPXC) I^2C Address 0x20–0x2A:

Monitor a variety of PMC bus signals;
Drive REDLED, YELLED, GRNALED;
Read SW1 switch pack, 4-bit board build code;
Select between BIOS Prom 0 and 1; Enable rear I/O RG mode (Merlin);
Verify PCI (33MHz to 132MHz) or PLD (14.318) clock is active;
Drive XMC MBISTH pin when STM controls JTAG loop;
Drive BUSMODE1 (currently disabled).

a193000p (Agate only) I^2C Address 0x30–0x3A:

Control access to CX2585 boot PROM and E4690's private LM63;
Select RGBHV input to ADV7441A between front and rear;
Enable E4690 TESTEN mode and JTAG mux (currently disabled);
Enable composite sync on green on VGA Ch 1 and 2;
Generate STANAG compatible sync (currently disabled);
Select CY22393 alternate clock set;
Enable VIN/CH 2 Green loopback test mode;
Read SW7 switch pack.

a194000p (All) I^2C Address 0x3C/0x3E:

Detect PMC and XMC and arbitrate power supply source;
Detect XMC 5V or 12V and if 12V, enable aux 12V to 5V switcher;
Enable multi-phase DC-DC switcher startup;
Drive FX3_LED (Agate), OTMP_LED, and OTEMP flag;
Drive VCORE voltage select;
Merlin only: Control front/rear DP Ch D and DP Ch C/D/F XMC/PMC;
Generate board master reset.

6.2.1 PLD Address Scan

You can use the on-board ISM software (see Section 6.3 for full details) to verify the PLD addresses:

ism> pld scan

AgatePXC		MerlinPXC		MerlinMTX	
PLD Addr	Typical Readback	PLD Addr	Typical Readback	PLD Addr	Typical Readback
20	00	20	00		
22	F3	22	F3		
24	D0	24	D0		
26	00	26	00		
28	39	28	39		
2A	E0	2A	E0		
30	01				
32	00				
34	00				
36	0F				
38	F0				
3A	FF				
3C	D0	3C	D0	3C	D0
3E	D0	3E	D0	3E	D0

The following pages provide the pinouts of each PLD and the associated CSR set.

6.2.2 Agate/MerlinMTX U012M6 LC4128ZE a192000p PLD

Table 6-1 Agate/MerlinMTX U012M6 LC4128ZE a192000p PLD

Port Name	Port Pin	I/O	PU/ PD	U012M6 Signal Name	Description
CK_3/I	88				
CK_2/I	39	CK	PU	PCI_CLK	Clock from PMC/PCI bus. 33MHz to 132MHz
CK_1/I	38	CK	PU	PLD_CLKR	Common clock for all PLDs: 14.318MHz
CK_0/I	89	I	PU	GPIO22_ROMCSB	BIOS ROM chip select from GPU
I_0	12	I	PD	STM_MBISTH	Asserted by STM to take over JTAG loop and tell XMC it did.
I_1	23				
I_2	27				
I_3	62	I	OFF	PERSTN	Master reset from XMC
I_4	73	I	OFF	PCI_RST_L	Master reset from PMC
I_5	77				
H6	84	I	PU	PCI_M66EN	Can be read in PLD CSR
H4	85	I	OFF	BUSMODE4_L	BUSMODE[4:1] should gate with PCI_RESET and reset board
H2	86	I	OFF	BUSMODE3_L	but many hosts don't do BUSMODE right so ignore for now
H0	87				
H13	78	I	PU	PXCRST_N	OR of PERSTN (XMC) and PCI_RST_L (PMC) bus resets
H12	79	I	PU	SW1_3	DIP SW1, bit 3. Can be read in PLD CSR
H10	80				
H8	81				
G2	72	I	PD	PMC_VDD_J2_36_R	Isolated VDD pin from PMC to tell if we are plugged in to PMC
G4	71	I/O	PU	GP_SDA	Board-wide I^2C
G5	70	I/O	PU	GP_SCL	Board-wide I^2C
G6	69	I	PU	SPARE_SWITCH	DIP SW2, bit 2. Can be read in PLD CSR
G8	67	I	PU	BIOS_SEL	DIP SW2, bit 1. Switch to select which BIOS PROM is active
G10	66	I	PU	SW1_6	DIP SW1, bit 6. Can be read in PLD CSR
G12	65	I	PU	SW1_5	DIP SW1, bit 5. Can be read in PLD CSR
G14	64	I	PU	SW1_7	DIP SW1, bit 7. Can be read in PLD CSR
F8	58	I	PU	SW1_2	DIP SW1, bit 2. Can be read in PLD CSR
F10	59	I	PD	VCC_PMC	Can be read in PLD CSR
F12	60	I	PU	SW1_4	DIP SW1, bit 4. Can be read in PLD CSR
F13	61	I	PU	SW1_8	DIP SW1, bit 8. Can be read in PLD CSR
F0	53				
F2	54				
F4	55				
F6	56				

E14	50				
E12	49				
E10	48	O	PU	PMC_RST_L	Reset 9X130 with local reset or hold reset on in XMC
E8	47				
E6	44	I	PD	PMC_VIO	Can be read in PLD CSR – another way to indicate PMC
E4	43				
E2	42				
E0	41	I	PU	PERST_L	Not used
D6	34	O	PU	SPARE	Line that goes to all PLDs and STM
D4	35	I	PD	BRDRST_N	Board-wide reset – generated by this PLD
D2	36	I	PU	INTD_L	
D0	37				
D13	28	O	PU	GRNALED_N	Wire-OR'd with 24T6 and STM. General purpose LED.
D12	29	O	PU	REDLED_N	Wire-OR'd with 24T6 and STM. General purpose LED.
D10	30	O	PU	YELLED_N	Wire-OR'd with 24T6 and STM. General purpose LED.
D8	31	O	PU	MBISTL	Use PLD driver gate to drive XMC line for STM
C2	22	I	PU	INTB_L	Can be read in PLD CSR
C4	21	I	PU	INTA_L	Can be read in PLD CSR
C5	20	O	OFF	BUSMODE1_L	see previous page.
C6	19	I	PU	INTC_L	Can be read in PLD CSR
C8	17				
C10	16	I	PU	SW1_1	DIP SW1, bit 1. Can be read in PLD CSR. RG_SEL on Merlin.
C12	15				
C14	14				
B8	8				
B10	9				
B12	10				
B13	11	I	PU	PMC_SOCKET	Flag indicates we are operating in a PMC (only) location
B0	3	I	PU	FORCE_XMC_12_N	DIP SW2, bit 3. Allow board to start up if VPWR=12V.
B2	4	I	PU	ROMCS1_N	Chip select for BIOS EEPROM #1
B4	5	I	PU	ROMCS0_N	Chip select for BIOS EEPROM #0
B6	6				
A14	100	I	PU	CD3	Build Code Bit 3 - Can be read in PLD CSR
A12	99	I	PU	CD2	Build Code Bit 2 - Can be read in PLD CSR
A10	98	I	PU	CD1	Build Code Bit 1 - Can be read in PLD CSR
A8	97	I	PU	CD0	Build Code Bit 0 - Can be read in PLD CSR
A6	94	I	OFF	VDD_18_OK	PLD needs to know that it has valid 1.8V to operate
A4	93				
A2	92				
A0	91	I	OFF	BUSMODE2_L	see previous page.

Table 6-2 a192000p Registers: I^2C Address 0x20–0x2A

0x20	**REG_0**	**DSW**	**Power up value: 00 (depends on switch settings)**
[7:0]	R only	SW[8:1]	DIP SW8 inputs – unallocated - could be used to define shipping configuration. Closed switch (on) reads high (1)

0x22	**REG_2**	**ICD**	**Power up value: F3 (depends on board build)**
[7:4]	R only	PCD[3:0]	PLD revision - count down from 1111b - coded in this PLD
[3:0]	R only	CD[3:0]	manufacturing build code - installed 0 ohm resistors read 0

0x24	**REG_4**	**PSW**	**Power up value: D0 (depends on system)**
[7:4]	R only	BUSMODE[4:1]_L	Valid only on PMC host - asserted reads (1)
[3:0]	R only	INT[D:A]_L	Valid only on PMC host - asserted reads (1)

0x26	**REG_6**	**SSW**	**Power up value: 00 (depends on switch settings)**
[7]	R only	BIOS_SEL	switch - "on" reads high
[6]	R only	SPARE_SWITCH	switch - "on" reads high
[5]	R only	FORCE_XMC_12_N	switch - "on" reads high. Switch must be on to enable board to operate in an XMC position with VPWR=12V.
[4:0]	not used	read back as 0	

0x28	**REG_8**	**MSW**	**Power up value: 39 (depends on system)**
[7]	R only	SPARE	High if board-wide “SPARE” line is high
[6]	R only	PCI_M66EN	High if PCI 66 MHz enabled on PMC slot
[5]	R only	PMC_VIO	High if PMC VIO (3.3 or 5V) is detected
[4]	R only	VCC_PMC	High if VCC (5V) detected on PMC bus
[3]	R only	PMC_VDD_J2_36	High if VDD (3.3V) is detected on PMC bus
[2]	R only	PCOUNT[23]	High if counter happens to have bit 23 set
[1]	R only	STM_MBISTH	High if STM is controlling board JTAG loop
[0]	R only	PMC_SOCKET	High if running on a PMC host

0x2A	REG_A	REGDATA	Power up/reset value: E0
[7]	R/W	GRNALED_N	high = LED on
[6]	R/W	YELLED_N	high = LED on
[5]	R/W	REDLED_N	high = LED on
[4]	R/W	PCOUNT_SEL	If in active PMC slot, use PCI_CLK instead of PLD_CLK for PCOUNT source,
[3]	R/W	BIOS_SW_EN_N	When low, allows BIOS_SEL dip switch off to select ROM#0 on to select ROM#1 (no ROM#1 installed) When high, allows regdata[2] low to select ROM#0, and high to select ROM#1 (no ROM#1 installed)
[2]	R/W	ROM_1_SEL	when high and regdata[3] = 1, select ROM#1
[1]	R/W	SPARE_DATEN_N	low allows serial data from this pld to drive SPARE (for debugging) high allows regdata[0] to drive SPARE
[0]	R/W	SPARE	when high and when regdata[1] = 1, drive SPARE high

6.2.3 Agate Only: U012C1 LC4256ZE a193000p PLD

Table 6-3 Agate Only: U012C1 LC4256ZE a193000p PLD

Port Name	Port Pin	Input/ Output	PU/ PD	U012M6 Signal Name	Description
CK_3/I	88	CK	PU	PLD_CLKR	Common clock for all PLDs: 14.318MHz
CK_2/I	39	I	PU	BRDRST_N	Master reset (from PLD U012M6)
CK_1/I	38			unused	
CK_0/I	89			unused	
I_0	12			unused	
I_1	23			unused	
I_2	27			unused	
I_3	62			unused	
I_4	73			unused	
I_5	77			unused	
P12	84	O	PU	CLK_SEL	Select CY22393 alternate clock set. Driven by SW_CLK_SEL
P10	85	O		FPG_CSYNC	Drive the VGA Ch 1 CSYNC mux
P66	86	I	OFF	HSYNC_DAC1	HSYNC/CSYNC from VGA Ch 1
P2	87	O		G_DAC_GND	Terminate VGA Ch 2 G on power up so loopback can work
O12	78	I/O	OFF	GP_SDA	Board-wide I^2C
O10	79	I/O	OFF	GP_SCL	Board-wide I^2C
O6	80			unused	
O2	81			unused	
N12	72	O		E_I2C_BUFEN	Enable GP I^2C to access E4690 private LM63
N10	71			unused	
N66	70			unused	
N2	69			unused	
M12	67			unused	
M10	66			unused	
M6	65	O		CX_I2C_BUFEN	Enable GP I^2C to access CX25858 private BIOS EEPROM
M4	64	O		TESTEN	Drive the E4690 TESTEN pin for JTAG testing
L12	58			unused	
L10	59	O		TS_JTAG_MUX	Enable E4690 JTAG onto board JTAG loop
L6	60			unused	
L4	61			unused	
K12	53			unused	
K10	54	I/O	PU	FP_RGB_SEL	Select between front/rear RGBHV inputs to ADV7441A
K6	55			unused	
K2	56			unused	

J12	50			unused	
J10	49			unused	
J6	48			unused	
J2	47			unused	
I12	44			unused	
I10	43			unused	
I6	42			unused	
I2	41			unused	
H12	34			unused	
H10	35			unused	
H6	36	I		STM_I2C_BUFEN	STM wants to access private devices
H2	37	I	PU	SW_I2C_BUFEN	DIP SW9, bit 1. Master enable for GP I^2C access to private
G12	28	I	PU	SW_CLK_SEL	DIP SW7, bit 8. Can be read in PLD CSR. Sel 22393 alt clks
G10	29			unused	
G6	30			unused	
G2	31			unused	
F12	22	I	PU	SW7_6	DIP SW7, bit 6. Can be read in PLD CSR
F10	21	I	PU	SW7_7	DIP SW7, bit 7. Can be read in PLD CSR
F6	20			unused	
F2	19	I	PU	SW7_5	DIP SW7, bit 5. Can be read in PLD CSR
E12	17	I	PU	SW7_4	DIP SW7, bit 4. Can be read in PLD CSR
E10	16	O		R_DAC_GND	Terminate VGA Ch 2 R on power up so loopback can work
E6	15	O		ADT_MUX_SEL	Enable VGA Ch 1 G to drive ADV G (loopback).
E4	14	I	PU	SW7_3	DIP SW7, bit 3. Can be read in PLD CSR
D12	8	O		CXT_MUX_SEL	Enable VGA Ch 2 Comp G to drive CX VIN8 (loopback)
D10	9	I	OFF	GPIO9_ROMSI	DIP SW7, bit 1. Can be read in PLD CSR. Enable VGA mode
D6	10			unused	
D4	11	I	OFF	GPIO5_AC_BATT	DIP SW7, bit 2. Can be read in PLD CSR. Reserved.
C12	3	O		B_DAC_GND	Terminate VGA Ch 2 B on power up so loopback can work
C10	4	O		TV_SEL_N	Select TV mode low pass filters
C6	5			unused	
C2	6	O		TVG_CSYNC	Drive the VGA Ch 2 CSYNC mux
B12	100			unused	
B10	99			unused	
B6	98			unused	
B2	97	I	OFF	HSYNC_DAC2	HSYNC/CSYNC from VGA Ch 2
A12	94			unused	
A10	93			unused	
A6	92			unused	
A2	91			unused	

Table 6-4 Agate Only: a193000p Registers: I²C Address 0x30–0x38

0x30	**REG0**	**DSW**	**Power up/reset value: 00**
[7]	R only	SW7_7	Enable VGA Ch 1&2 Composite Sync (GPU must be set too)
[6]	R only	SW7_6	Enable ADT and/or CX MUX select bits (PCS[3:2])
[5]	R only	SW7_5	Enable E4690 JTAG and TESTEN to work
[4]	R only	SW7_4	Enable VGA Ch 2 low pass filters
[3]	R only	SW7_3	Enable VGA Ch 2 DAC GNDs for loopback testing,
[2]	R only	GPIO9_ROMSI	DIPSW VGA enable
[1]	R only	GPIO5_AC_BATT	DIPSW E4690 Perf Select (doesn't seem to do anything)
[0]	R only	SW_CLK_SEL	DIPSW input pin select alternate timing set in CY22393 to drive CLK_SEL HIGH to select alternate set. ALT_CLK_SEL (ICD[2]) can programmatically set CLK_SEL.

0x32	**REG2**	**PCS**	**Power up/reset value: 00**
[7:4]	n/a	not used	
[3]	R/W	ADT_MUX_SEL	PCS[3] = swap VGA Ch 1 Green into ADV G/SOG input. Used to implement video loopback test of ADV7441A. SW7_3 must be On.
[2]	R/W	CXT_MUX_SEL	PCS[2] = swap VGA Ch 2 Blue/CPS into CX25858 V8 input. Used to implement video loopback test of CX25858. SW7_3 must be On.
[1:0]	n/a	not used	

0x34	**REG4**	**ICD**	**Power up/reset value: 00?** **N**ot tested yet
[7]	R/W	PCSYNCEN	Enable VGA Ch 1 SyncOnGreen. SW7_7 force enables SOG
[6]	R/W	SCSYNCEN	Enable VGA Ch 2 SOG. SW7_7 force enables SOG
[5]	n/a	not used	
[4]	R/W	TV_BW_SEL	Controls muxes that pass VGA Ch 2 DAC output through low pass (TV) or high pass (RGB) bandwidth filters. clear for VGA (high pass) filter on secondary video output set for TV (low pass) filter on secondary video output SW7_4 forces low pass filter select.
[3]	n/a	not used	

[2]	R/W	ALT_CLK_SEL	HIGH to select CY22393 alternate clock set - if CY not programmed with an alternate set then board will not work.
[1]	R/W	PIO_FP_RGB_SEL	IF SW9 1-2 is open, select front panel RGBHV for input to ADV. If SW9 1-2 is closed, it overrides PIO_FP_RGB_SEL
[0]	R only	SW_FP_RGB_SEL	Direct read of the FP_RGB_SEL pin. If PIO_FP_RGB_SEL is high and SW_FP_RGB_SEL is low, then SW9 1-2 is closed

0x36	**REG6**	**not used**	**Power up/reset value: FF**

0x38	**REG8**	**regdata**	**Power up/reset value: FF?**
[7:4]	R only	PCD[3:0]	PROM revision code - count down from 1111b
[3]	R/W	JTAG_MUX_EN	Allow JTAG mux to switch 4690 into JTAG loop. Need to set SW7_5 on as well.
[2]	R/W	E_I2C_BUFEN	If SW7_6 is on, setting E_I2C_BUFEN will gate E4690 private LM63 (0x98) onto GP I^2C bus.
[1]	R/W	CX_I2C_BUFEN	If SW7_6 is on, setting CX_I2C_BUFEN will gate CX private PROM (0xA0) onto GP I^2C bus.
[0]	R/W	TESTEN	Set TESTEN high to enable E4690 JTAG mode. Use I^2C access to disable E4690 PCIe clock on 011H5 (ICS9DB403D) and GPU Clock from CLKB on U011D4 (CY22393). SW7_5 and JTAG_MUX_EN must be set as well. Care must be taken in putting E4690 into JTAG mode. For example, AMD says chip can overheat if GPU and PCIe clocks are not properly disabled.

0x3A	**REGA**	**not used**	**Power up/reset value: FF**

6.2.4 Agate/Merlin U012H4 LC4064ZE PLD

Table 6-5 Agate/Merlin U012H4 LC4064ZE PLD

Port Name	Port Pin	Input/ Output	PU/ PD	U012M6 Signal Name	Description
CK_3/I	42	CK	PU	PLD_CLKR	Common clock for all PLDs: 14.318MHz
CK_2/I	19	I	PU	SW_P23M_N	DIP SW4, bit 2. ON selects x8 lane operation on GPU side.
CK_1/I	18				
CK_0/I	43	I	PU	PXCRST_N	OR of PERSTN (XMC) and PCI_RST_L (PMC) bus resets
D0	41			XMC_5	Enable power from VPWR when it is 5V
D2	40			VCC_XMC_OK	VCC OK from auxiliary 12V to 5V switcher
D4	39			VDD_18_OK	Goes high when all switchers are up and running
D6	38			GPIO15_CPWR_1	Bit 1 of VCORE select. Driven by GPU or CSR
D8	34			GPIO17_THERMINT_L	Interrupt to/from GPU signaling overtemp
D10	33			OTMP_LED_N	Drive the front panel Red OTEMP LED on
D12	32			VDD_CORE_START	Start up the multi-phase DC-DC switcher system
D15	31			PMC_SOCKET	**Agate/MerlinPXC**: Enable power from PMC 5V. **MTX:** n/c
C11	28			GPIO19_CTF	Flag from GPU that die sensor has detected overtemp
C10	27			GPIO20_CPWR_2	Bit 2 of VCORE select. Driven by GPU or CSR
C8	26			FX3_LED_N/PORT_SEL	**Agate**: FX3 LED. **Merlin**: PMC/XMC DP select **MTX:** n/c
C6	24			GPIO21_BB_EN	**Agate/MerlinPXC**: n/c **MTX:** VDDR1 = 1.35/1.5V
C4	23			P01M_N	Control signal to 24T6 to select x4 (high) or x8 (low) on host
C2	22			SW_P01M_N	DIP SW4, bit 1. ON selects x8 lane operation on host side.
C1	21			P6_SEL	**Merlin**: front/rear DP Ch D select
C0	20			P23M_N	Control signal to 24T6 to select x4 (high) or x8 (low) on GPU
B0	17			FORCE_XMC_12_N	DIP SW2, bit 3. Allow board to start up if VPWR=12V.
B2	16			BRDRST_N	Master reset (from PLD U012M6)
B4	15			GP_SCL	Board-wide I^2C
B6	14			GP_SDA	Board-wide I^2C
B8	10			PMC_VDD_J2_36_R	**Agate/MerlinPXC**: Isolated PMC VDD **MTX**: Spare Sw Input
B10	9			LM75_OTMP_N	Interrupt from LM75 that it has an overtemp event
B12	8			GPIO6_MPWR_0	**Merlin only**: VDDCI select. Driven by GPU or CSR
B15	7			GPIO16_CPWR_0	**Merlin only**: Bit 0 of VCORE select. Driven by GPU or CSR
A11	4			XMC_12_PWR	From voltage detectors – XMC VPWR has valid 12V
A10	3			SPARE	Line that goes to all PLDs and STM
A8	2			XMC_ANY_N	From voltage detectors – XMC VPWR has valid 5V or 12V
A6	48			XPERR_RSTN_OC	From voltage detectors - power error detected!!!!!
A4	47			PMC_SOCKET_N	Force XMC detectors off when in PMC power mode
A2	46			XMC_12	Enable power gate to pass power from aux 12V to 5V switcher
A1	45			VCC_XMC_ENBL	Enable auxiliary 12V to 5V switcher
A0	44			XMC_5_PWR	From voltage detectors – XMC VPWR has valid 5V

Table 6-6 a194000p Registers: I²C Address 0x3C-0x3E

0x3C	REG0	PSR (Read only)	Power up/reset value: xx
[7:4]	R only	PCD[3:0]	PLD revision code - currently 1101b
[3]	R only	XMC_ANY	High if we are in XMC mode
[2]	R only	XMC_12_PWR	HIGH for XMC = 12V detected. SW2-3 must be set to allow board to run when VPWR=12V.
[1:0]	R only	SW_P[23:01]M	DIP SW4 bits [1:0] force E4690 PCIe port to run in x8 mode - XMC only. 24T6 determines the merge setting on the trailing edge of system reset. Selecting x4 instead saves power.

0x3E	REG0	DSW	Power up/reset value: E0
[7:5]	R/W	**Agate:** CPWR_[2:0] Measured voltage at E4690 is about 5mV lower due to IR drop across board.	**Agate:** CPWR_2 CPWR_1 CPWR_0 VCORE 1 1 x 0.90V 1 0 x 0.95V 0 1 x 1.00V 0 0 x 1.056V
		Merlin: CPWR_[2:0] Measured voltage at E8860 is about 5mV lower due to IR drop across board.	**Merlin:** CPWR_2 CPWR_1 CPWR_0 VCORE 1 1 1 0.980V 1 1 0 0.955V 1 0 1 0.930V 1 0 0 0.905V 0 1 1 0.880V 0 1 0 0.855V 0 0 1 0.830V 0 0 0 0.805V
[4]	R/W	**MerlinPXC:** P6_SEL **MerlinMTX:** VDDR1 **Agate:** not defined	**MerlinPXC:** DP Ch C/D/F PMC/XMC select: high = XMC **MerlinMTX**: high for VDDR1 = 1.35V
[3]	R/W	**Merlin:** GPIO6_MPWR_0 **Agate:** not defined	**Merlin:** CPWR_0 VCORE 1 0.900V 0 0.950V
[2]	R/W	CMPWR_READ_MODE	When set, reads actual CPWR and MPWR GPU bus bits. When clear, reads PLD internal bits. This is important because the GPU usually controls the CPWR and MPWR bits, and if they are driven low, the PLD and override them. So, before trying to use the CPWR and MPWR PLD bits, set CMPWR_READ_MODE. If any of the CPWR and MPWR bits are 0, then don't try to use the PLD bits.
[1]	R/W	OTEMP_LED_ON	Force the OTEMP_LED on and blinking. Testing only.
[0]	R/W	**Agate:** FX3_LED_N **Merlin:** PORT_SEL	**Agate:**Set FX3 LED on **Merlin:** front/rear DP Ch D select. High = rear.

6.3 STM32F427 Integrated System Monitor (ISM)

6.3.1 Overview

The ST Micro STM32F427 is based on the high-performance ARM Cortex-M4 32-bit RISC core operating at 180 MHz. It incorporates 2MB Flash and 256 KB SRAM.

The Integrated System Monitor (ISM) code is built on the ChibiOS open source RTOS. One of the features of this OS is that there is very little in the way of a basic OS command structure. Thus, virtually all of the commands in ISM are unique to ISM.

ISM starts automatically on power-up, having been loaded into STM flash during the manufacturing process. It is possible to update the flash using procedures documented in Chapter 7.

6.3.2 Integrated System Monitor Command Summary

The subsequent sections document the commands in order.

Global Command Modifiers

loop

Help Command

help

Informational Commands

info	mem	systime	threads	uptime	ver

Operational Commands

adv	cfr	cx	dipsw	exit	freq
hid	i2c	jtag	led	pld	scan
sho/show	temp	vcore	volts	vpd	

Unsupported Commands

flash	gpu	reset

Firmware Update

DfuSe: firmware upgrade STMicroelectronics extension

6.3.3 Global Command Modifiers

loop Preface a command with *loop* to repeat the command until the ESC key is pressed.

| separates 2 possible commands (logical OR)

6.3.4 Help Command

help *help* lists all the commands for which there is help information

Example:

```
ism> help
adv, cfr, cx, dipsw, exit, freq, gpu, help, i2c, info, jtag, led,
loop, mem, pld, reset, scan, show, systime, temp, threads,
uptime, vcore, ver, volts, vpd
```

help command, where *command* is the one you want to know about.

Example:

```
ism> help jtag
jtag reset -- reset JTAG chain
tag scan  -- scan JTAG chain
```

6.3.5 Informational Commands

info prints out *info*rmation about the ChibiOS RTOS, ST processor specifications, and platform that the ISM is running on

Example:

```
ism> info

Kernel:         2.7.0unstable
Compiler:       GCC 4.4.1
Architecture:   ARMv7-ME
Core Variant:   Cortex-M4
Port Info:      Advanced kernel mode
Platform:       STM32F427 High Performance with DSP and FPU
Board:          Rastergraf Merlin
Build time:     Mar 2 2016 - 09:37:16
```

mem Report ISM memory allocations

Example:

```
ism> mem
core free memory: 170400 bytes
heap fragments: 0
heap free total: 0 bytes
```

systime Report ISM system usage time in milliseconds

Example:

```
ism> systime
401493
```

threads Report ISM thread allocations

Example:

```
ism> threads
      name       addr      stack   prio  refs     state time
      main  200010CC  200007A4     64     1  SLEEPING 701
      idle  20001118  20001194      1     1     READY 412585
 heartbeat  20002880  2000293C     64     1  SLEEPING 0
 uart-shell  20001A00  20001ACC     64     1  SLEEPING 0
     shell  200044F8  2000547C     64     1  WTQUEUE 0
usb_lld_pump  200015C8  20001694      2     1     READY 1
usb-serial  200029B8  20002A7C     64     1  SLEEPING 0
   usb-hid  20003808  200038D4     64     1  SLEEPING 0
   measure  20002518  200025D4     64     1  SLEEPING 0
       icu  20002740  200027FC     64     1  SLEEPING 0
     shell  200055B0  200064D4     64     1  CURRENT 4
```

uptime Report ISM system usage time in milliseconds

Example:

```
ism> uptime
Rastergraf Merlin, up 0 days, 0:11:37
```

ver Report the current version of ISM

Example:

```
ism> ver
Merlin 00.20.0022
```

6.3.6 Operational Commands

adv **Agate:** Initialize the ADV7441A

Usage:

adv cvbs Initialize the ADV7441A for composite video capture on AIN1.

adv svga Initialize the ADV7441A RGB video capture on AIN1-3.

Example:

ism> adv cvbs

cfr **Agate:** Force reset of CX3, FX3 and ADV7441A
MerlinPXC: Force reset of CX3.

Usage:

cfr [l [time]]

Command drives the reset pin low for approx 2ms. If "l" is specified, that means loop and do continual resets. If time is included, then that's the loop time (>= 25ms, default 1000ms).

Example:

ism> cfr

cx **Agate, MerlinMTX:** Access the CX25858 boot PROM.

Usage:

cx [e|i|l|p|t [cnt]|v|[addr] /]

cx e erase PROM

cx i report PROM device type

cx l write standard boot code hardcoded in ISM into PROM.

cx p print contents of PROM

cx t <cnt> test <cnt> bytes of PROM

cx v <cnt> verify erased <cnt> bytes of PROM

cx <addr/> examine address <addr> in the PROM

Example:

cx l

dipsw **Agate, MerlinPXC**. Read 8-bit dipswitch connected to PLD1.

Example:

ism> dipsw

PLD1_0: dipsw = 0x00

exit exit ISM and restart the ST processor

Example:

ism> exit

ChibiOS/RT Merlin Shell
ism>

freq Measure the vertical and horizontal frequencies of video sources.

VGA channels must be actively displaying graphics in order for the frequencies to be measured.

The ADV7441A must have an active video input source.

1 = VGA Ch 1.

2 = VGA Ch 2. **Agate only**.

3 = V/H inputs to ADV7441. **Agate only**.

Example:

ism> freq 1

Channel 1: Vfreq = 56.30 Hz, Hfreq = 60.100 kHz

hid Enable the ISM to connect to a keyboard or mouse and act like a terminal. Requires that the gpu command also work.

Example:

ism> hid

i2c Operate on local I^2C devices. You can scan for I^2C devices present on the graphics board and read and modify registers in the I^2C device. I^2C applies to both I^2C or SMBus devices.

Modifiers:

w	specify to perform double wide (16-bit) data operations
value	8-bit or 16-bit quantity to be deposited in selected register
reg	register to be accessed
idev	specify the device to be accessed – see following table

Usage:

i2c scan|reset|quiet
i2c idev [reg] [w] value|/

i2c scan	scan I^2C bus for devices
i2c reset	reset I^2C bus
i2c quiet	stop periodic I^2C activity
i2c idev [w] value	write value into single register device
i2c idev [w] /	read from single register device
i2c idev <reg> [w] value	write value into multiple register device
i2c idev <reg> [w] /	read from multiple register device

Example:

ism> i2c pld1_0 ff	write ff into pld1 reg 0

idev	I2C Address	Part Number	Comment	Description
pld1_n	0x20/2/4/6/8/A	PLD 1	n = 0, 2, 4, 6, 8, or A	PLD (Agate, MerlinPXC)
pld2_n	0x30/2/4/6/8/A	PLD 2	n = 0, 2, 4, 6, 8, or A	PLD (Agate)
pld3_n	0x3C/E	PLD 3	n = C or E	PLD on all boards
vd7441	0x42/6/A/E	ADV7441A	ADV7441A reg set 1	DVI/RGBHV Digitizer (Agate)
ics1526	0x4C	ICS1526	Agate Rev 1 only	
vd7441	0x62/6/A/E	ADV7441A	ADV7441A reg set 2	DVI/RGBHV Digitizer (Agate)
gp4690	0x82	E4690 GPU		GPU on Agate
gp8860	0x82	E8860 GPU		GPU on Merlin
lm75	0x90	LM75		Power Supply Thermal sensor
s1015	0x92	ADS1015		Ancillary 4 Ch A/D
lm63	0x98	LM63		GPU Thermal sensor
cxeepr	0xA0	BR24T02	I2C_BUF_EN must be set	2Kb Boot PROM for CX25858
stmeepr	0xA8	24LC256		256Kb VPD EEPROM
px9130	0xC0/2	PCI7C9X130	active only in PMC host	PCIe to PCI bridge
pc22393	0xD2	CY22393		Master clock
clock	0xDC	ICS9DB403		PCIe clock driver
switch	0xEE	IDTHPES24T6G2		PCIe switch

jtag Scans the jtag capable devices. Normally, GPU is excluded from JTAG loop but it can be enabled for special testing modes.

Usage

jtag reset	reset JTAG chain
jtag scan	scan JTAG chain
jtag gscan	scan JTAG chain including GPU (not implemented)

Example:

```
ism> jtag scan                  [for Merlin]

JTAG chain report:
0x808104C2                      [M4128ZE]
0x08C820FE                      [9X130]
0x146007E6                      [24T6G2]
0xE0490696                      [CX3]
0x800107C2                      [M4064ZE]

JTAG scan found 5 devices in chain.
```

led set the red, amber, & green LEDs on the top long edge of the board and the error LED on the front panel.

Usage:

led	read status of LEDs
led red|grna|er|amb|all on|off	turn a specific LED on or off
[loop] led banner p|s|t|a	turn on LEDs in unique sequence for PLD (p), STM (s) or 24T6 (t); (a) to cycle all modes. Adding “loop” cycles until you hit ESC. **(p) doesn’t apply on MerlinMTX.**

Example:

```
ism> led
red: off, grna: off, er: on, amb: off
```

pld use instead of I^2C command to access PLD

Modifiers:

reg, idev, w, and value as defined in **i2c** command

Usage:

pld idev value	write pld register
pld idev /	read pld register
pld scan	scan I^2C bus for known plds

Example:

ism> pld pld1_0 /	(read PLD1, reg 0)

scan scan devices

Usage:

scan pld	search for pld 1, 2, and 3 (same as “pld scan”)
scan i2c	search for all I^2C devices (same as “i2c scan”)
scan jtag	search for jtag devices (same as “jtag scan”)

Examples:

```
ism> scan jtag
JTAG chain report:
0x808104C2      M4128ZE
0x08C820FE      9X130
0x146007E6      24T6G2
0xE0490696      CX3
0x800107C2      M4064ZE
JTAG scan found 5 devices in chain.
```

(Examples continue following page)

ism> scan i2c	search for I^2C and smb devices on Agate
pld1_0 @ 0x20	
pld1_2 @ 0x22	
pld1_4 @ 0x24	
pld1_6 @ 0x26	
pld1_8 @ 0x28	
pld1_a @ 0x2A	
pld2_0 @ 0x30	
pld2_2 @ 0x32	
pld2_4 @ 0x34	
pld2_6 @ 0x36	
pld2_8 @ 0x38	
pld2_A @ 0x3A	
pld3_0 @ 0x3C	
pld3_2 @ 0x3E	
vd7441 @ 0x42	
vd7441_1 @ 0x46	
vd7441_3 @ 0x4A	
ics1526 @ 0x4C	Agate Rev 1 only
vd7441_4 @ 0x4E	
vd7441_2 @ 0x62	
vd7441_6 @ 0x66	
vd7441_5 @ 0x6A	
vd7441_7 @ 0x6E	
lm75 @ 0x90	
ads1015 @ 0x92	
ismeepr @ 0xA8	
lm63 @ 0x98	
px9130 @ 0xC0	shows only on PMC
px9130_1 @ 0xC2	shows only on PMC
pc22393 @ 0xD2	
ics9db4 @ 0xDC	
switch @ 0xEE	
bus 0: 32 devices found	

(Examples continue following page)

ism> scan i2c	search for I^2C and smb devices on Merlin

```
pld1_0 @ 0x20
pld1_2 @ 0x22
pld1_4 @ 0x24
pld1_6 @ 0x26
pld1_8 @ 0x28
pld1_a @ 0x2A
pld3_0 @ 0x3C
pld3_2 @ 0x3E
gp8860 @ 0x82
lm75 @ 0x90
ads1015 @ 0x92
lm63 @ 0x98
ismeepr @ 0xA8
px9130 @ 0xC0          shows only on PMC
px9130_1 @ 0xC2        shows only on PMC
pc22393 @ 0xD2
ics9db4 @ 0xDC
switch @ 0xEE
bus 0: 18 devices found
```

show Search for devices. See **i2c** section of **idev** information

Modifiers:

reg, idev, w, and value as defined in **i2c** command

Usage:

```
show i2c idev [reg] [w]|pld idev|dipsw|freq|leds|temp|ver|volts
show i2c idev                    show single register device
show i2c idev reg                show reg in multi register device
show pld idev                    show single register in a pld
show dipsw                       show dipswitch in PLD1_0
show freq chan                   show freq ch 1, 2, or 3
show leds                        show state of leds
show temp                        show temp sensors
show version                     show ICM version
show volts                       show voltage test points
show vpd [sn|mod|assy|fxvdd]     show vpd parameters
```

Example:

```
ism> show dipsw          show dipswitch in PLD1_0

PLD1_0: dipsw = 0x00
```

temp Report temperature at various locations:

Device	Location
lm75	Side 1 between PMC connectors
lm63	Side 1 near GPU
diode	Side 1 inside GPU
asic	read of GPU thermal ctrl register
stm	Side 1 near front panel

Example:

ism> temp

lm75 = 31.12C, lm63 = 37C, diode = 52.62C, asic = 46.0C, stm = 30.3C

vcore test GPU vcore voltage levels. It will not be possible to run this test if GPU has control of vcore control lines

Usage:

vcore test
vcore set vset

Example:

ism> vcore test

E8860 has control of CPWR - skipping test

vpd load Vital Product Data into STM auxiliary EEPROM.

Usage:

vpd [init|sn|mod|assy|fxvdd] [value]

vpd	write all parameters step by step
vpd init	erase EEPROM
vpd sn	write serial number
vpd mod	write model number
vpd assy	write assembly number
vpd cxvdd	write measured CX3 VDD value – used to calibrate STM A/D converters

Example:

ism> vpd

Enter the Vital Product Data at the prompts.
Serial Number [sn]: (etc)

volts Report voltage test points

Example:

```
ism> volts
```

Signal	ADC	Expected	Measured	
STM_VDDCI	ADC123_IN1	0.90/0.9545V	0.944V	[GPU VCORE I/O]
STM_VDD_095	ADC123_IN2	0.955V	0.940V	[General]
STM_CX_VDDIO	ADC123_IN3	3.3V	2.886V	[CX3 VIO]
STM_VDD_18	ADC12_IN8	1.8V	1.787V	[General]
STM_VDD_C	ADC12_IN9	0.805-0.980V	0.845V	[GPU VCORE]
STM_VDD_10	ADC123_IN10	1.0V	1.040V	[General]
STM_VDD_25	ADC123_IN11	2.5V	2.467V	[General]
STM_VDD_12C	ADC123_IN12	1.2V	1.210V	[CX3 VCORE]
STM_VDD_R1	ADC123_IN13	1.362/1.508V	1.490V	[GPU Memory]
STM_VDDR3	ADC12_IN14	3.3V	3.302V	[General]
STM_VFP	ADC12_IN15	0.0/3.3V	3.323V	[MIPI Supply V]
VCC	ADS1015_3	5.0V	4.908V	[General]
XSEN	ADS1015_0	1.5-2.5A	0.006A	(see note)

Note: The VCC Current is a good indication of power consumption of the board because all of the DC-DC converters run on the local VCC. Also, the 3.3V current usually doesn't exceed 0.5A. The VCC Current signal name itself changes depending whether the board is running on a PMC or XMC host: it reads PSEN for PMC, XSEN for XMC (VPWR = 5V), or TSEN for XMC (VPWR = 12V).

Unfortunately, the current sensing chip is both VCC and temperature sensitive. It may not read correctly if VCC is relatively high or the board temperature is relatively low. If it reads 0.006A, as shown in the example (above), it is NOT working. It should read at least 1.5A.

6.3.7 Unsupported Commands

flash *flash prog*, specifies that a new ST ISM firmware image "prog" is to be downloaded into the ST processor.

Not Implemented.

Use the ST Micro DFU firmware update procedure instead.

gpu *gpu, u*sing AtomBIOS, initialize and activate with a default 800x600 format any gpu display channel found to be connected to a monitor

gpu init, as above, but using a predefined init table:

Init	Format
1	1280x1024
2	1600x1200

Not Implemented.

This command should be used only on PowerPC systems that otherwise cannot initialize the graphics board and must not be used on x86 systems that have a system BIOS.

reset *reset* the STM32F427 chip and restart the ISM.

Not Implemented.

Just use the reset button on the board. A reset command would still be useful to have when running a remote console.

6.4 Thermal and Voltage Sensors

As mentioned in Section 6.3, the Agate and Merlin boards are well instrumented for both voltage and temperature.

The temperature sensors include:

Device	Location
LM75	Side 1 between PMC connectors in the power supply section
LM63	Side 1 near GPU
Diode	is actually inside the GPU. Read by LM63 or GPU control registers
ASIC	Separate thermal sensor inside GPU, read via GPU control registers
STM	Side 1 near front panel

The voltage sensors include

Device	Voltages and Currents Monitored
STM	8-11 major system voltages (depending on board)
ADS1015	1x voltage, 3x current (but current values not always reliable)

The easiest way to monitor the temperature and voltage values is using the ISM console program and access via a terminal emulator program.

However, the LM75, LM63, and GPU-based thermal sensors are also accessible via the board's unified I^2C bus and thus ***could*** also be read through the 24T6 GPIO port using a "software I^2C" protocol. The addresses for the devices can be found in Section 2.5.3. This is not supported as yet.

The LM75 is a single sensor device and as used on the Agate and Merlin boards, monitors the temperature in the power supply area. It has a default over-temperature alert that is set to 70°C.

The LM63 is a dual sensor device, having a local sensor like the LM75 and a remote 2-wire diode sensor connected to a thermal diode in the GPU. There are separate over-temperature alerts for the each sensors, each set to 70°C.

Because of its location, the GPU diode runs a hot even under normal conditions, so its over-temperature defaults must be set higher to avoid spurious error reporting. To that end, the ISM firmware reprograms the "set point high" threshold to 90°C and the set point critical to 95°C.

When either the LM75 or LM63 detects an over-temperature state, the front panel red LED is lit and an interrupt is generated to the ISM firmware.

The ASIC thermal sensor is part of the GPU's register set and is programmed very much like the LM75.

There isn't "backdoor" way to get to the voltage and current functions. You have to go through the ISM. It would be possible to write a script to interrogate the ISM via its USB port, but that support is not yet available.

6.5 Non-volatile Memories

There are a number of non-volatile memories on the boards:

PROM Size and Type	Part Number	Purpose	Boards	Programmer
2Kb, I^2C	BR24T02	CX25858 Boot PROM	Agate, MerlinMTX	ISM firmware
2Kb, I^2C	BR24T02	XMC VPD	All	TBD
256Kb, I^2C	24LC256	24T6 Boot PROM	All, but not installed	n/a
256Kb, I^2C	24LC256	ISM VPD PROM	All	ISM firmware
1Mb, SPI	M25P10	GPU Video BIOS	All	AMD Windows app
1Mb, SPI	M25P10	uPD720201 Boot PROM	Agate, MerlinPXC	Renesas Windows app
4Mb, SPI	M25P40	CX3 Control Store PROM	Agate, MerlinPXC	Cypress Windows app
4Mb, SPI	M25P40	FX3 Control Store PROM	Agate	Cypress Windows app
2Mb, SWM	STM32F427	STM Firmware Flash	All	STM Windows app
PLD, JTAG	LC4128ZE	PLD_1 - a192000p	Agate, MerlinPXC	Lattice Windows app
PLD, JTAG	LC4256ZE	PLD_2 - a193000p	Agate	Lattice Windows app
PLD, JTAG	LC4064ZE	PLD_3 - a194000p	All	Lattice Windows app

Please see Chapter 7 for information about how to program these devices.

Note that it isn't possible for any Agate or Merlin on-board device to save image data from on-board graphics memory. Also, when power is removed, all image data stored in the graphics memory disappears..

Chapter 7
On-Board Device Programming Procedures

7.1 Board Programming Procedures

Several devices must programmed prior to using the board in a live system.

A bare PMA-P or PME-P carrier connected to 3.3V and 5V supplies can be used as a test fixture. A fan is also required to blow air on the board. See Section 7.2 (PMA-P) or 7.3 (PME-P) for instructions on how to set up the carrier board.

Table 7-1 Programming Procedures Summary

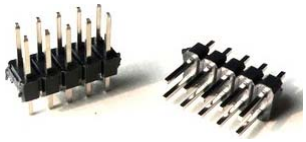
Step	Section	Device(s)	Agate/Merlin Application	Programming Method	Manufacturing Stage
1	n/a	CY22393	Master Clock Generator	Cypress CY3672 programmer w/CY3698 adapter and Cypress Windows-based s/w.	Pre-assembly Can be temporarily reprogrammed via I^2C.
2	7.2	PMA-P	Test Fixture for Agate or MerlinPXC	n/a	Prior to use in system.
2	7.3	PME-P	Test Fixture for MerlinMTX	n/a	Prior to use in system.
3	5.5, 5.6, 5.7	Switches and Jumpers	operating settings	n/a	Prior to use in system.
4	2.9	Power and Clocks	system checks	n/a	Prior to use in system.
	5.13	LEDs			
6	7.4	Graphics Board	Install board on test fixture	n/a	Prior to use in system.
5	7.5	STM32F427	Integrated System Monitor (ISM)	Use PMA-P or PME-P fixture. Agate/Merlin SWD Debug connector to ST-Link/V2 Pod and ST Windows-based s/w.	Prior to use in system.
6	7.6	LC40xxx PLDs	Board CSRs and logic	Use PMA-P or PME-P fixture with Lattice HW-DLN-3C Parallel Port Cable and Lattice Windows-based ispVM s/w. Lattice USB cable won't work	Prior to use in system.
7	7.7	CX25858	Boot PROM	Use PMA-P or PME-P fixture. ISM firmware command	Prior to use in system.
8	7.8	E4690 (Agate) or E8860 (Merlin)	BIOS PROM	Agate or Merlin is used as **secondary** display controller. Use AMD E4690 atiwinflash utility in Admin Command Prompt window for both boards. E8860 atiwinflash is broken.	In active system.
9	7.9	uPD720201	Boot PROM	Renesas Windows utility.	In active system.
10	7.10	CX3 or FX3	Boot PROM	Cypress Windows utility.	In active system.

7.2 Setting up a PMA-P as a Test Fixture

The initial steps for setting up an Agate or MerlinPXC must be done in a no-OS environment. One way to do this is to use a Rastergraf PMA-P. **Note that you need a PME-P for the MerlinMTX** – see Section 7.3.

You can order a prepared board from Rastergraf: PMA-P/TF

Or, you can do it yourself. You will need the following items (header, switch, and fan links are to ***suggested*** parts at Digikey):



a) Rastergraf PMA-P board, without P2 connector

b) 3.3V@3A and 5V@6A power supplies (a typical PC Supply would work)

c) 2x5 header: Harwin M20-9980545

d) 10K 1/8W resistor

e) 10uF, 6.3V capacitor

f) momentary-on pushbutton switch: C&K TP11SHZBE

g) 5V, 28CFM fan: Delta Electronics AFB0805L

h) wires, tools, etc.

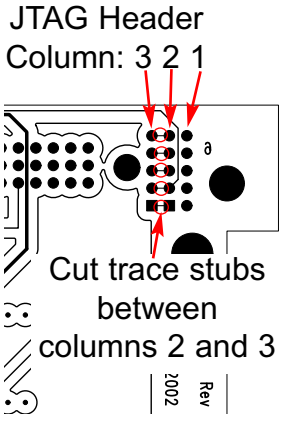
Note that the changes you make will render the PMA-P unusable as a normal PMC/PCI carrier board.

7.2.1 Cut the traces on the back of the PMA-P

Modify the JTAG header pin array to disconnect the trace links between the second and third columns of pins:

Flip the PMA-P over to show the back (solder) side. Orient the board with the PCB gold card edge connector closest to you. Locate the JTAG header holes in the upper right corner. VERY CAREFULLY cut the 5 little stub traces between Columns 3 and 2. DO NOT CUT the long trace going to the pad in Column 2.

Figure 7-1 Back side of PMA-P Showing Traces to be Cut

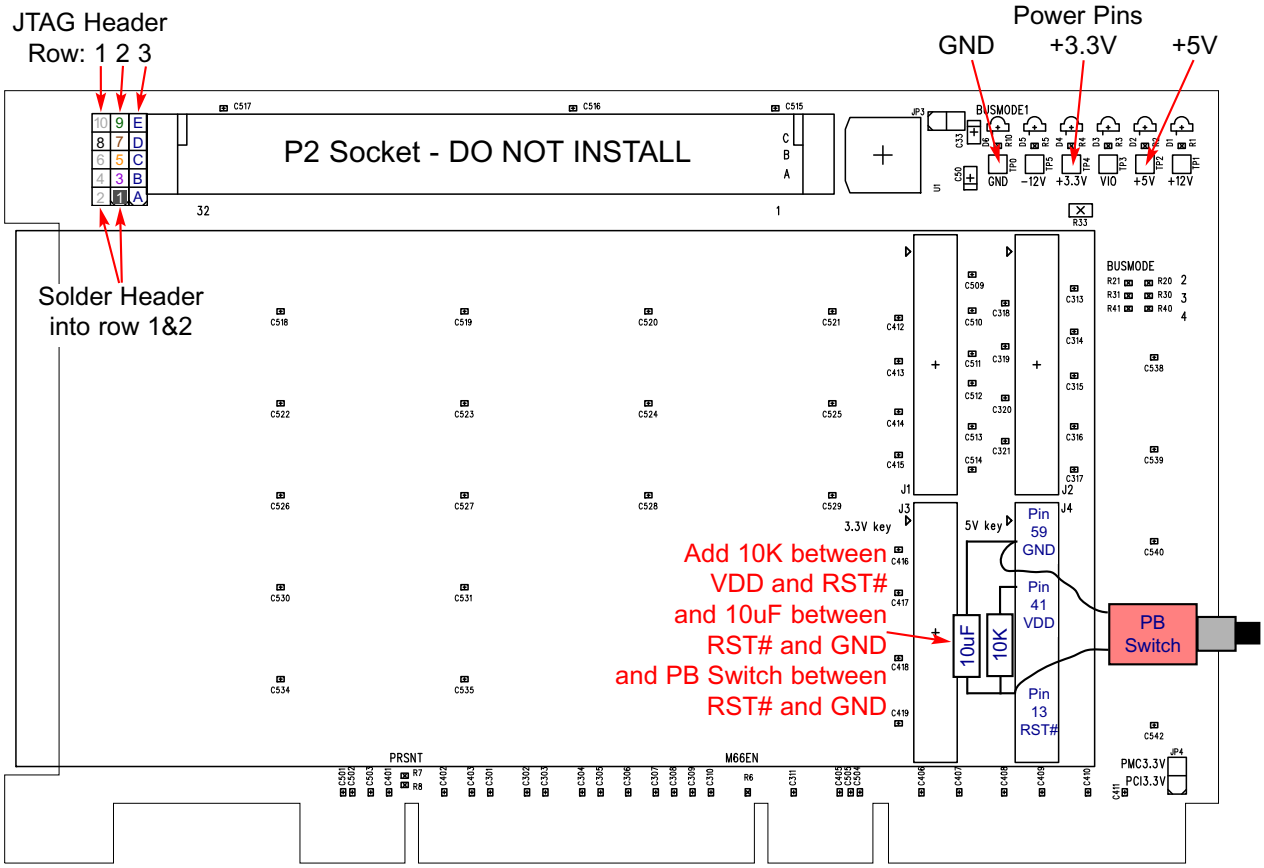


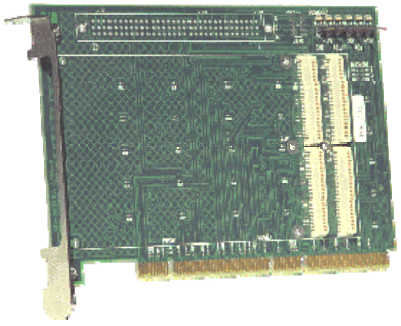
<< Back side of PMA-P

7.2.2 Install header. switch, pullup, and capacitor

1) Solder in a 2x5 0.1” WW header into columns 1 and 2 of the JTAG array;
2) if necessary, solder in pins into the GND, 3.3V, and 5V holes;
3) solder a 10K between pin 41, VDD, and pin 13, RST# pin;
4) solder a 10uF between pin 59, GND, and pin 13, RST# pin;
5) solder a pushbutton switch between pin 59, GND, and pin 13, RST# pin.

Figure 7-2 Modifications to PMA-P



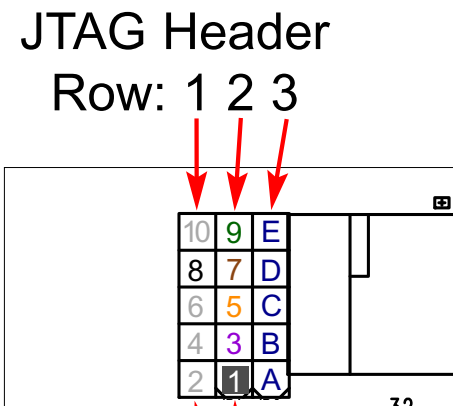


7.2.3 Connect Lattice Download Cable to PMA-P JTAG Header

Connect the Lattice HW-DLN-3C Download Cable to PMA-P JTAG Header using the table and figure below as guides:

Table 7-2 Connect Lattice HW-DLN-3C Download Cable to PMA-P JTAG Header

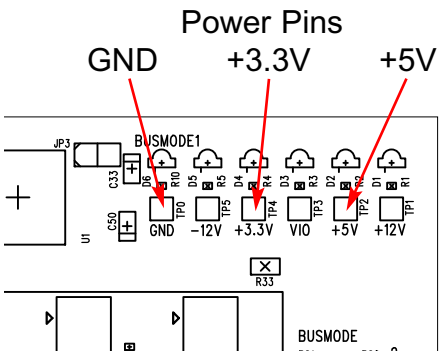
Signal	PMA-P JTAG Header	HW-DLN-3C Download Cable Lead	
Name	Pin	Pin	Color
PMC_TRST#	9	TRST	Green
PMC_TDO	7	TDO	Brown
PMC_TDI	5	TDI	Orange
PMC_TMS	3	TMS	Violet
PMC_TCK	1	TCK	White
GND	8	GND	Black
	wire from PMA-P VDD power pin to one end of 4.7K	other end of 4.7K to VCC	Red



7.2.4 Connect the Power Supplies to the PMA-P power pins

Securely connect the 3.3V and 5V power supplies to the PMA-P power pins as shown below. ***After doing this, check all connections and voltages***.

Figure 7-3 Power Connections to the PMA-P



7.3 Setting up a PME-P as a Test Fixture

The initial steps for setting up a MerlinMTX must be done in a no-OS environment. One way to do this is to use a Rastergraf PME-P. **Note that you need a PMA-P for the Agate or MerlinPXC** – see Section 7.2.

You can order a prepared board from Rastergraf: PME-P/TF

Or, you can do it yourself. You will need the following items (header, switch, and fan links are to ***suggested*** parts at Digikey):

a) Rastergraf PME-P board

b) 3.3V@3A and 5V@6A power supplies
(a typical PC Supply would work)

c) 2x5 header: Harwin M20-9980545

d) 5V, 28CFM fan: Delta Electronics AFB0805L

e) wires, tools, etc.

Note that the changes you make will render the PME-P unusable as a normal XMC/PCI carrier board.

7.3.1 Trace cuts and parts changes

Cut traces as shown below

Figure 7-4 Back Side of PME-P Showing Traces to be Cut

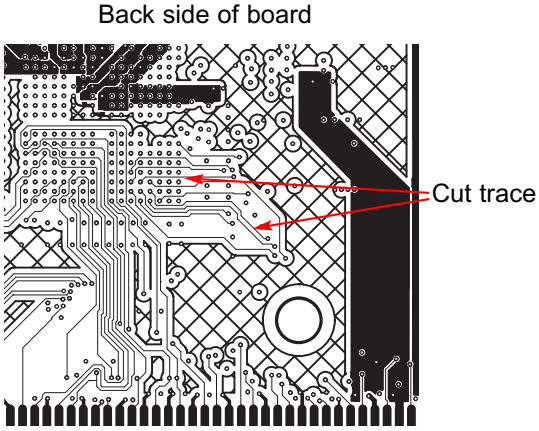
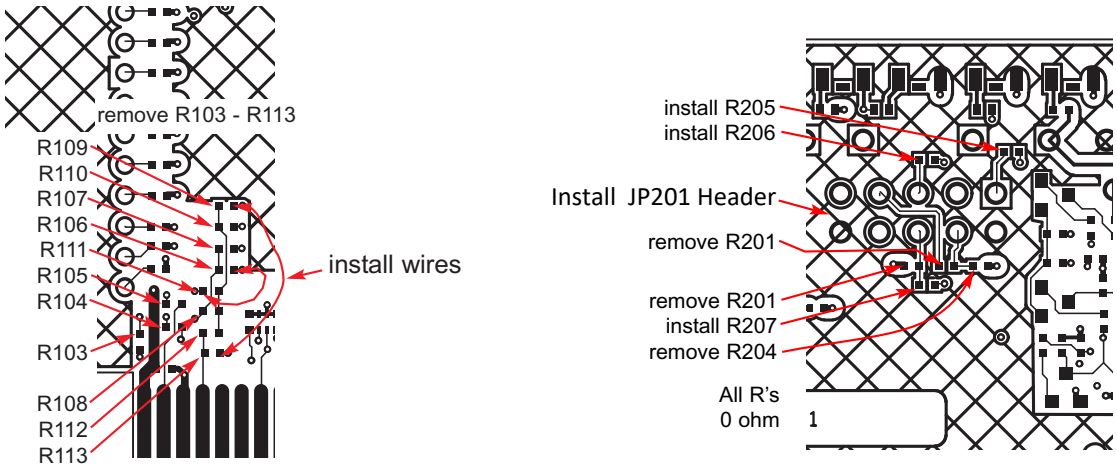


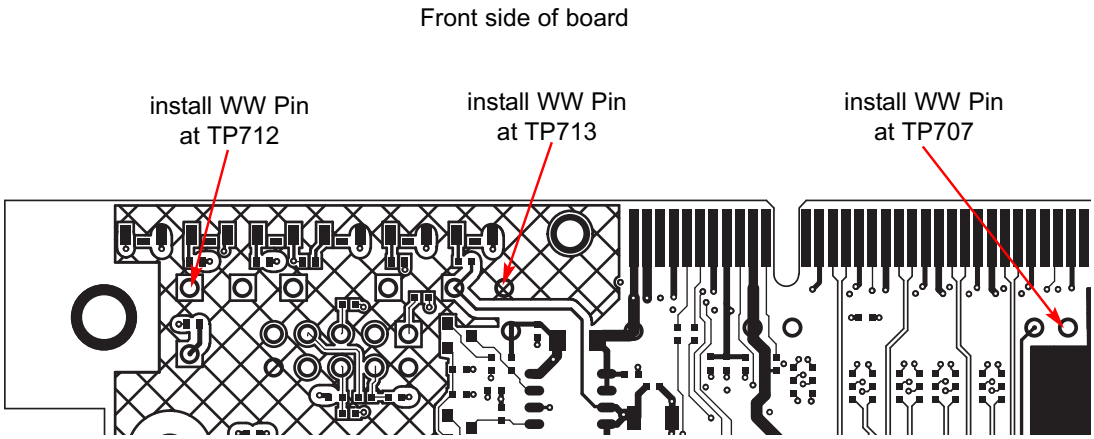
Figure 7-5 Front Side of PME-P Showing Parts to be Changed



7.3.2 Install header and pins.

1) Solder in a 2x5 0.1" WW header as shown at JP201 (see diagram above);
2) Solder single WW pins at TP712, TP713, and TP707 (see diagram below);

Figure 7-6 PME-P WW Pin Installation



In addition:

3) remove jumper at JP501 7-8

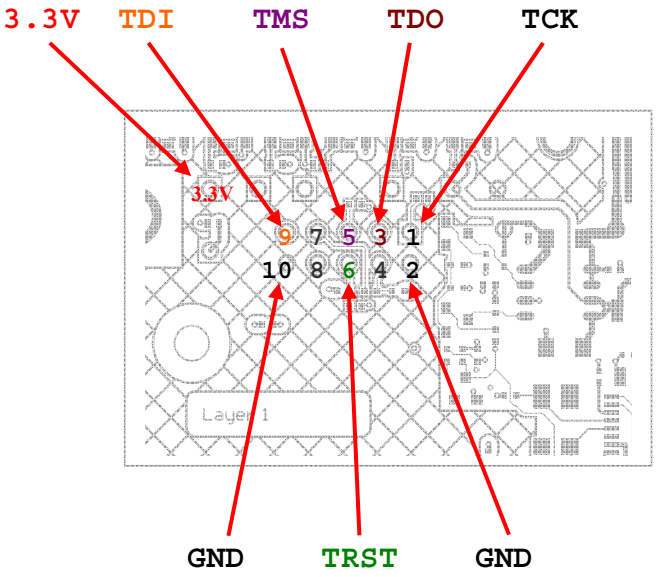
4) install jumper at JP504 2-3

7.3.3 Connect Lattice Download Cable to PME-P JTAG Header

Connect the Lattice HW-DLN-3C Parallel Download Cable to PME-P JTAG Header using the table and figure below as guides. Do not use a Lattice USB cable – it won't work.

Table 7-3 Connect Lattice HW-DLN-3C Parallel Port Download Cable to PME-P

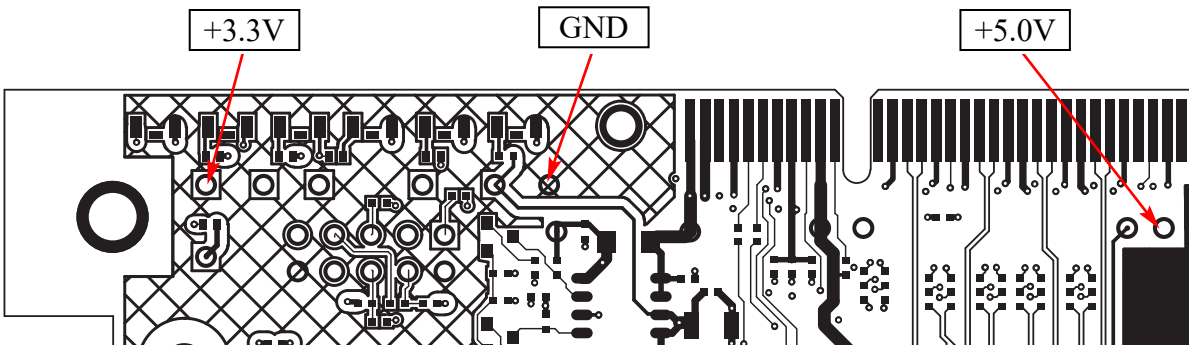
Signal	PMA-P JTAG Header	HW-DLN-3C Download Cable Lead	
Name	Pin	Pin	Color
PMC_TCK	1	TCK	White
PMC_TDO	3	TDO	Brown
PMC_TMS	5	TMS	Violet
PMC_TDI	9	TDI	Orange
PMC_TRST	6	TRST	Green
GND	2, 10	GND	Black
VCC	wire from PME-P 3.3V power pin to one end of 4.7K	other end of 4.7K to +3.3V	Red



7.3.4 Connect the Power Supplies to the PME-P power pins

Securely connect the +3.3V and +5V power supplies to the PME-P power pins as shown below. ***After doing this, check all connections and voltages***.

Figure 7-7 Power Connections to the PME-P



7.4 Install the Graphics Board on the Prepared Carrier

7.4.1 Install the Agate or MerlinPXC Graphics Board on the PMA-P

It is assumed that the Agate or MerlinPXC you are working with is a known good working unit. If it isn't, then **stop**: only Rastergraf or Rastergraf-trained technicians should attempt to work with a board that has never been powered-up before.

a) Set SW3-2 ON to bypass power sequencing control to enable initial start

b) Verify that all other switch settings follow Section 5.5 (Agate) or Section 5.6 (MerlinPXC)

c) Plug the board into the PMA-P and make sure that all the connections to the Download Cable and the power supplies and fan are secure;

d) power up the PMA-P/graphics board set;

e) make sure that the fan is blowing air on the board, preferably aimed at the section of the board closer to the front panel;

   If you don't have a fan, again, **stop** and go no further. You **WILL** fry the board if you have no fan blowing air on it;

f) Proceed to Section 7.5.

7.4.2 Install the MerlinMTX Graphics Board on the PME-P

It is assumed that the MerlinMTX you are working with is a known good working unit. If it isn't, then **stop**: only Rastergraf or Rastergraf-trained technicians should attempt to work with a board that has never been powered-up before.

a) Set SW1-8 ON to bypass power sequencing control to enable initial start

b) Verify that all other switch settings follow Section 5.7 (MerlinMTX)

c) Plug the board into the PME-P and make sure that all the connections to the Lattice Download Cable and the power supplies and fan are secure;

d) power up the PME-P/graphics board set;

e) make sure that the fan is blowing air on the board, preferably aimed at the section of the board closer to the front panel;

   If you don't have a fan, again, **stop** and go no further. You **WILL** fry the board if you have no fan blowing air on it;

f) Proceed to Section 7.5.

7.5 Program the STM32F427

It is assumed that the board is already installed on a PMA-P or PME-P as per Section 7.4. If not, please follow the instructions there before proceeding.

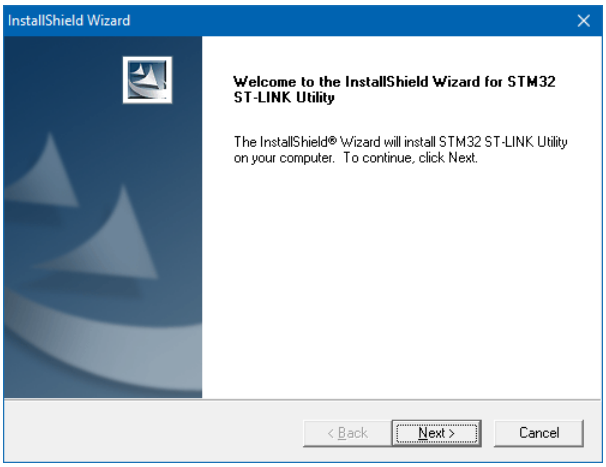
7.5.1 Obtain an ST-LINK/V2 and Cable

Follow the procedures in Section 3.10.1 to obtain an ST-LINK/V2 and build the cable to connect between the ST-LINK/V2 and the J012C6 Agate or Merlin SWD-DP Debug connector. If you don't want to build the cable, you can order one from Rastergraf.

7.5.2 Install the ST-LINK/V2 Software

a) Use the CD provided with the ST-LINK/V2 or use this link to the relevant ST web page to download the current version. Be sure to select the signed driver version. You will have to set up an account on the ST website before you can download the code.

Figure 7-8 ST-LINK Utility Software Screen Shot #1



If you get an error of the form:
1608: Unable to load instance InstallDriver,
Try this:

Rename the InstallShield folder
In Windows Explorer or in My Computer, open the following folder:
DRIVE \Program Files\Common Files\
Right-click the Installshield folder, and then click Rename.
Type InstallShield1, and then press ENTER.
Run the install again.
If it still fails, go to this link and try the other solutions.

7.5.3 Program the Image into the STM32F427

a) Contact Rastergraf for the current memory image for your board. The file name will be something like merlinMTX-427_v0.20.27-fscomm.hex.

b) Once you have installed the ST-LINK/V2 software, plug the pod into a USB port. Windows will eventually see that you have done this and report that it has installed the USB driver for the ST-LINK/V2;

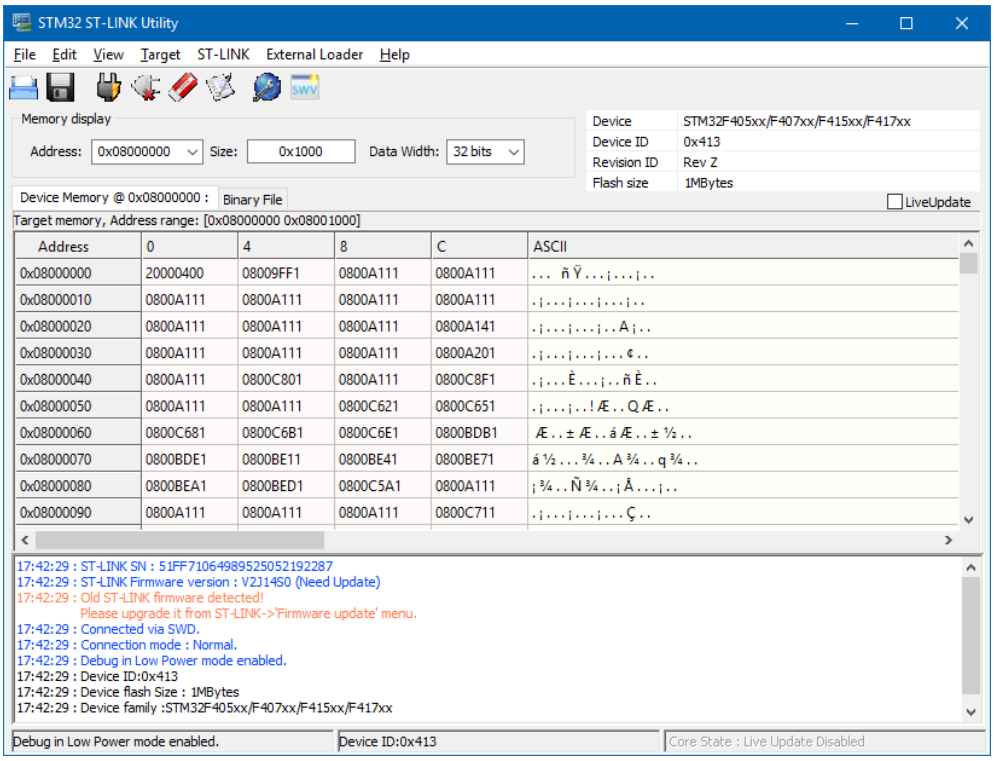
c) Connect the ST-LINK/V2 pod to the Agate or Merlin using the cable previously built in Section 3.10.1;

d) Power up the carrier/board set. A fan must be blowing on the board set;

e) Verify that the LED on the pod is lit, alternating red and green;

f) Run the ST-Link software. The software should bring up a popup and show the status as it locates and connects to the CPU on the Rastergraf board. If for some reason it doesn't do this, go to the Target tab in the software and select Connect. It should connect. If it tries and fails, you most likely have a cable problem.

Figure 7-9 ST-LINK Utility Software Screen Shot #2

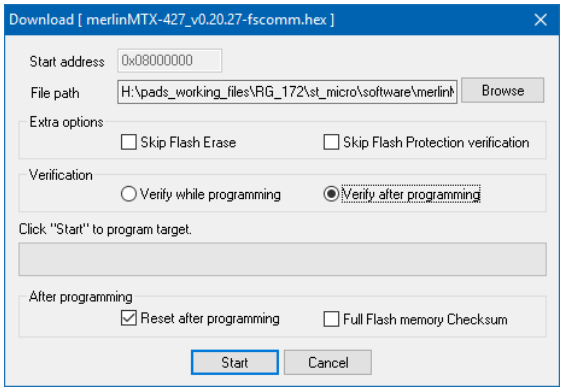


g) Select Target, then Program & Verify

h) Select the hex image you want to program

i) Get the following popup:

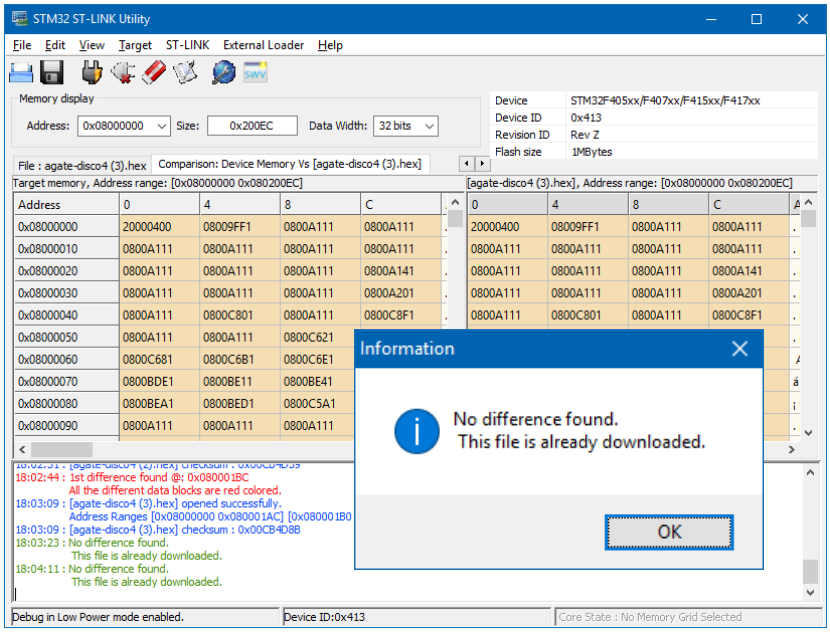
Figure 7-10 ST-LINK Utility Software Screen Shot #1



j) be sure to specify Verify after programming. You should get a success report.

k) You can also do a compare

Figure 7-11 ST-LINK Utility Software Screen Shot #3



l) Exit the program.

7.6 Program the PLDs

The following table show what PLDs are used on the boards. In all cases, the actual PLD code is the same for a given PLD on any board. Refer to Section 6.2 for details about how the PLDs are used.

Table 7-4 PLD Utilization by Board Model

PLD Part Number	Agate	MerlinPXC	MerlinMTX
a192000p	yes	yes	no
a193000p	yes	no	no
a194000	yes	yes	yes

7.6.1 Install the ispVM Software

The PLDs a re Lattice LC4000ZE devices. They are programmed using the Lattice ispVM software. You will have to set up an account on the Lattice website before you can download the code. You also have to request a (free) license from Lattice for the software and it is tied to your computer's Ethernet board.

You will also need to obtain the PLD files and Agate or Merlin chain file from Rastergraf. **Do not attempt to create and use your own files or you could irreparably damage the board.**

Figure 7-12 ispVM Screen Shot #1

7.6.3 Connect the Program Cable

As noted before, you have to use the Lattice HW-DLN-3C Parallel Download Cable. For reasons not yet understood, the USB-based cable will not work.

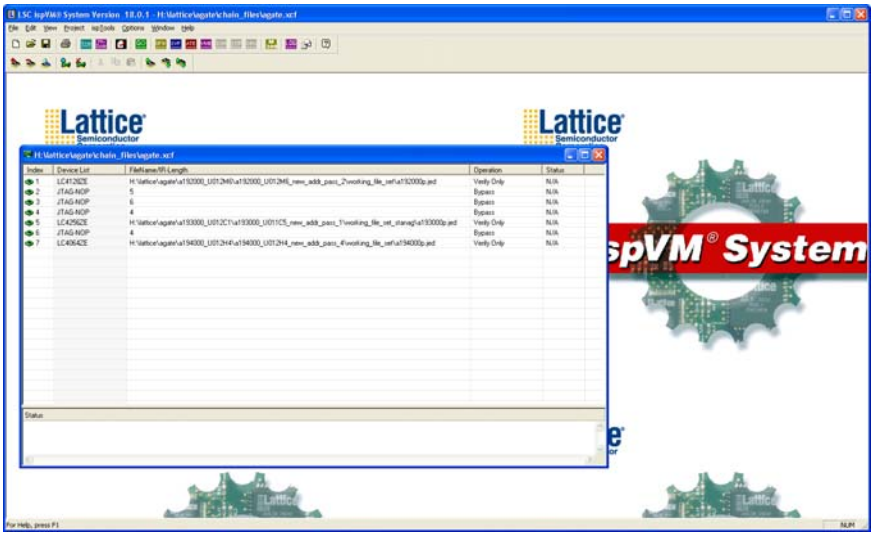
Please see Section 7.2.3 (Agate/MerlinPXC) or Section 7.3.3 (MerlinMTX) for instructions on how to connect the cable.

7.6.3 Program the PLDs

a) start up ispVM;

b) load the chain file: **File > Open > agate.xcf (or merlin.xcf)**;

Figure 7-13 ispVM Screen Shot #2



c) go to **Project > Project Settings > Advanced** and set TCK Low Pulse Width Delay to 5.

d) Set the chain file for Verify ID: **Edit > Set Chain Operations > Verify ID**

e) Select: **Project > Check Configuration Setup**

If this fails, look at the error log and try to fix the problem. **Until you get a clean Check Configuration Setup you cannot proceed.**

f) Once you do pass, **Edit > Set Chain Operations > Erase, Program, Verify**

This sets the chain file to program all of the PLDs. If you only want to program one PLD at a time, edit the chain file entries accordingly.

Also, the names of the files as shown in the chain file example above may not be the files you receive from Rastergraf. Be sure to change the files names to mach before proceeding with the programming.

g) If you get a pass on all parts, you are done. If not, something is broken and you need to contact Rastergraf.

7.7 Program the CX25858 Boot PROM (AgatePXC, MerlinMTX)

Use the ISM command:

cx **Agate, MerlinMTX:** Access the CX25858 boot PROM.

Usage:

cx [e|i|l|p|t [cnt]|v|[addr] /]

cx e	erase PROM
cx i	report PROM device type
cx l	write standard boot code hardcoded in ISM into PROM.
cx p	print contents of PROM
cx t <cnt>	test <cnt> bytes of PROM
cx v <cnt>	verify erased <cnt> bytes of PROM
cx <addr/>	examine address <addr> in the PROM

Example:

ism> cx l	write standard boot code hardcoded in ISM into PROM

7.8 Program the E4690 or E8860 VBIOS PROM

AMD provides DOS (atiflash) and Windows (atiwinflash) versions of the VBIOS program. Since the programs are available only under NDA from AMD, contact Rastergraf to obtain a copy. You will also need the VBIOS image itself which is ONLY available from Rastergraf.

It is possible to edit certain parts of the VBIOS using the Atomworks and PowerPlay programs. Editable functions relevant to the Rastergraf boards include GPU and memory clocks and voltages and output port assignments, activity, and output mode. The Graphics Output subheading in Section 2.3 (Agate), 2.4 (MerlinPXC), and 2.5 (MerlinMTX) lists the output assignments for each board. Please contact Rastergraf if you are interested in modifying the VBIOS.

7.8.1 VBIOS Program using DOS

Create a bootable DOS USB thumb drive using this link:

https://www.thomas-krenn.com/en/wiki/Creating_a_Bootable_DOS_USB_Stick

It does everything, including building the boot record and even supplies a correct freedos image so you don't have to find that either. A truly useful piece of software.

Once you have created the thumb drive image, copy over the atiflash program and the BIOS image on to the thumb drive, shut down Windows, and boot to the thumb drive.

Then, enter the following command:

For Agate:

atiflash –st –f –fp –fs –fm –fa –p[a or 1]* BR43743.104

For MerlinPXC:

atiflash –st –f –fp –fs –fm –fa –p[a or 1]* ECET1148.005.BIN

For MerlinMTX:

atiflash –st –f –fp –fs –fm –fa –p[a or 1]* ECET1148.006.DP_2DVI.BIN

* use 1 in an dual-Rastergraf-board system

You should get a successful completion message and be told to reboot. Remove the thumb drive and reboot. You should have a functioning Rastergraf board now. If you have never had a Rastergraf board in your system Windows will eventually complain that it needs a proper driver. See Chapter 8 for information about that.

7.8.2 VBIOS Program using Windows

Note: testing has shown that the E8860 atiwinflash Version 2.6.1 does not work correctly. Please use the E4690 atiwinflash Version 2.0.1.18 instead

Startup an Administrator Command Window.

CD to the directory where you have atiwinflash and the VBIOS image.

Then, enter the following command:

For Agate:

atiwinflash –st –f –fp –fs –fm –fa –p[a or 1]* BR43743.104

For MerlinPXC:

atiwinflash –st –f –fp –fs –fm –fa –p[a or 1]* ECET1148.005.BIN

For MerlinMTX:

atiwinflash –st –f –fp –fs –fm –fa –p[a or 1]* ECET1148.006.DP_2DVI.BIN

* use 1 in an dual-Rastergraf-board system

You should get a popup with a successful completion message, some information about the PROM image, and a message to reboot.

Once rebooted, you should have a functioning Rastergraf board. If you have never had a Rastergraf board in your system Windows will eventually complain that it needs a proper driver. See Chapter 8 for information about that.

7.9 Program the uPD720201 Firmware (AgatePXC, MerlinMTX)

This section only applies to the AgatePXC and MerlinPXC. The MerlinMTX doesn't have a USB controller.

Renesas does not willingly provide copies of either the device-specific driver nor the BIOS code for the uPD720201.

However, there is a public website that usually has the latest versions of both. Please refer to Section 8.4 for the driver information.

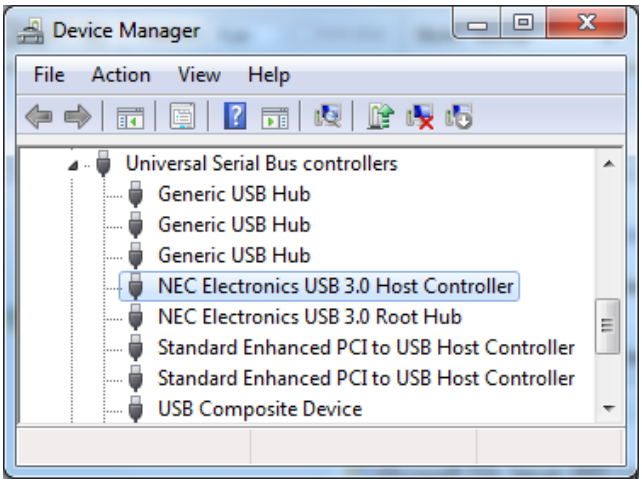
There are 2 versions of the BIOS that are in current use and it seems that some people have better results with one than the other.

Renesas/Nec uPD720201/720202 USB 3.0 Firmware Version 2.0.2.4

Renesas/Nec uPD720201/720202 USB 3.0 Firmware Version 2.0.2.6

Before embarking on a firmware change, make sure that the Windows driver for the uPD720201 is installed - see Section 8.4 for details on how to install the driver. With the MerlinPXC graphics board plugged in, you can check to see if the driver is already installed by going to Device Manager, open the USB Devices. You should see something like this:

Figure 7-14 uPD720201Firmware Screen Shot #1



7.9.1 Firmware Programming Example

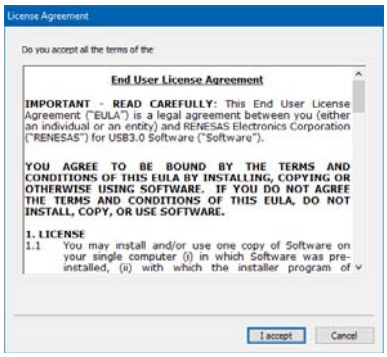
Here is a sample update procedure from the Renesas 2.0.2.6 readme:

a) Disconnect all USB devices connected with the USB3.0 ports.

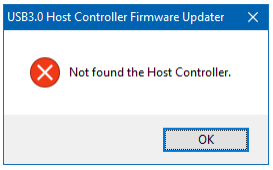
b) Execute "K2026FWUP1.EXE".

c) Show the License Agreement. If you accept the terms , select "I accept".

Figure 7-15 uPD720201Firmware Screen Shot #2

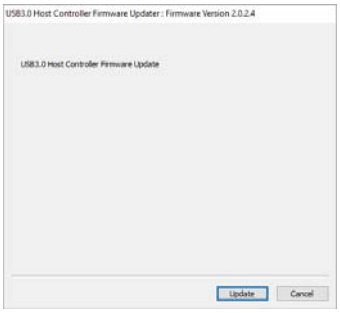


If you get the following:



And yet the graphics board is plugged in, you have a hardware problem with the board. Instead, you should get:

Figure 7-16 uPD720201Firmware Screen Shot #3



d) Press "Update" button.

e) After updating, restart the computer.

7.9.2 Programming Failure Recovery Procedure

Sometimes the uPD720201 update may fail. In this case, here is how to proceed:

a) re-download 2.0.2.4 version

b) Start K2024FWUP1.exe, but don't click update

c) Go to Windows temp folder and check for a folder named IXP000.TMP

d) Copy the folder anywhere, open it and edit the file W201FWup.ini:

    [Option]
    Version=1
    to
    [Option]
    Version=0

    this will force reapply the downgrade to 2.0.2.4

e) Start W201FWUP.exe for 64 bit system or W201FWUP_x86.exe for 32 bit systems

After restart you can try to reapply the 2.0.2.6 upgrade

7.10 Program a CX3/FX3 SPI PROM (AgatePXC, MerlinMTX)

The CX3 and FX3 are part of the Cypress family of SuperSpeed USB peripheral controllers. They share many of the same programming tools and programs. The CX3 is a special version of the FX3 that has been customized to support MIPI CSI-2 cameras.

In order to do anything with the FX3 or CX3 you have to first install the Cypress Development Suite, as described in Section 8.7.

There is a CX3 on both the AgatePXC Rev 2 and the MerlinPXC. The FX3 is only on AgatePXC Rev 2. The MerlinMTX doesn't have either device.

On the Agate or MerlinPXC, the CX3 or FX3 can be configured to start from power up in one of two modes:

a) boot from USB (only) or

b) SPI PROM first/USB on SPI fail:

AgatePXC – FX3 uses SW8 to select between (a) and (b);

AgatePXC – CX3 uses SW10 to select between (a) and (b);

MerlinPXC – CX3 uses SW8 to select between (a) and (b).

In the default selected mode, the CX3 or FX3 looks to its associated boot PROM (SPI PROM) for a startup program. If the PROM is erased, then it boots via USB, and, assuming that the Cypress drivers have been correctly installed, a program can be loaded into the CX3 or FX3 RAM or SPI PROM using Cypress Control Center program.

To make it easy to see if the CX3 or FX3 is working, Rastergraf preloads the associated SPI PROM with a simple "Blinker" program that blinks the activity LED connected to the CX3 or FX3. If you press the reset switch on the board, it will reset the FX3 and/or CX3 and cause the chip to go back to the "Blinker" program (unless you have overwritten the SPI PROM with your own program).

You could download your own program into SPI PROM, which will wipe out the Rastergraf program, but we advise that instead you download your program into RAM, and it will automatically start once the download has completed.

If you accidentally erase the "Blinker" program, change the affected chip's SW8 or SW10 to force the chip to boot from USB and then use the Cypress Control Center to reload the program. Contact Rastergraf and we can send you the "Blinker" image.

The following procedure will show you how to reload the "Blinker" program in the SPI PROM. Of course, you can use this procedure to load any program into SPI PROM.

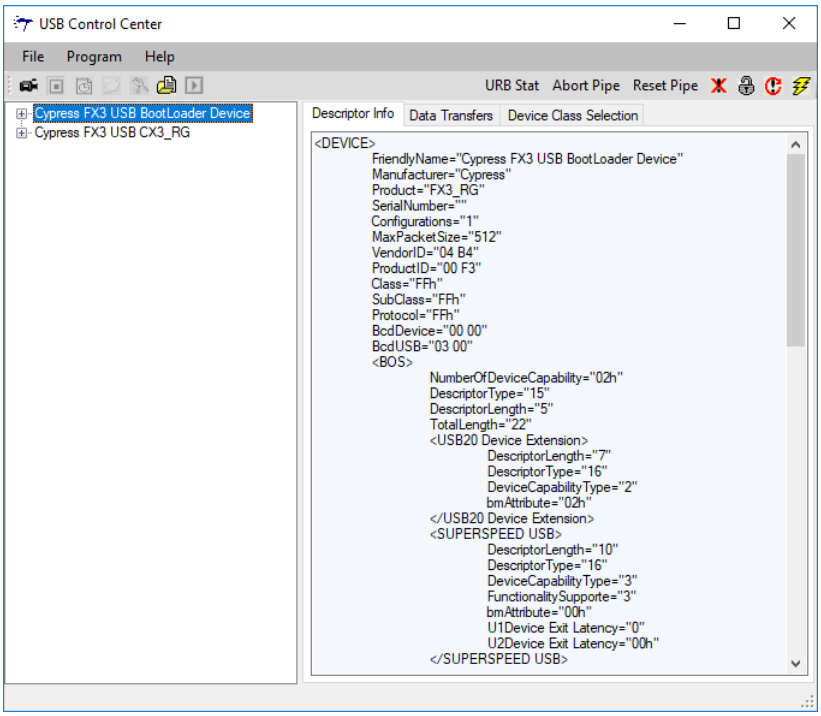
7.10.1 Program the Blinker Program into the FX3 or CX3

Before doing anything else, please make sure that you have followed the procedure in Section 8.4 to install the uPD720201 driver (for XP-W7) as well as the procedures in Section 8.8.1 to install the Cypress SDK and USB driver set.

Until and unless you can see the CX3 and/or FX3 in Device Manager as shown in Figure 8-8 you will not be able to proceed further. If you don't, then you have to get that fixed before going further.

Assuming all is well, then start up the Cypress USB Control Center. You should have a screen like the figure below. Notice that both devices are actually running the standard Cypress Bootloader program even though the second line doesn't say so. See Section 2.6.4 for more information.

Figure 7-17 Cypress USB Control Center Screen Shot



If you have both CX3 and FX3, highlight the correct chip in the left hand column. Then, select Program, the memory you want to program, browse to the image, and select OK.

Chapter 8
System Software

Rastergraf

8.1 Introduction

This chapter covers the software that is needed to use the Agate or Merlin in a typical operating system (OS) environment: There are several chips on the various boards that need to be considered from the OS standpoint:

Table 8-1 On-Board Devices Requiring Operating System Software

Device	Manufacturer and Part Number	Applicable Boards	Software Supplier
PCIe Switch	IDT 89HPES24T6G2	All	OS, IDT
PCIe to PCIe Bridge	Pericom PI7C9X130	AgatePXC, MerlinPXC	OS, Rastergraf
USB Host Controller	Renesas uPD720201	AgatePXC, MerlinPXC	OS
Graphics controller	AMD E4690	AgatePXC	AMD
	AMD E8860	Merlin (all)	AMD
8 Ch A/V Digitizer	Conexant CX25858	AgatePXC, MerlinMTX	Rastergraf
MIPI Controller	Cypress CX3	AgatePXC, MerlinPXC	Cypress, Rastergraf
Digital Video In	Cypress FX3	AgatePXC	Cypress, Rastergraf
In System Monitor	ST Micro STM32F427	All	ST Micro, Rastergraf

This chapter has the following sections:

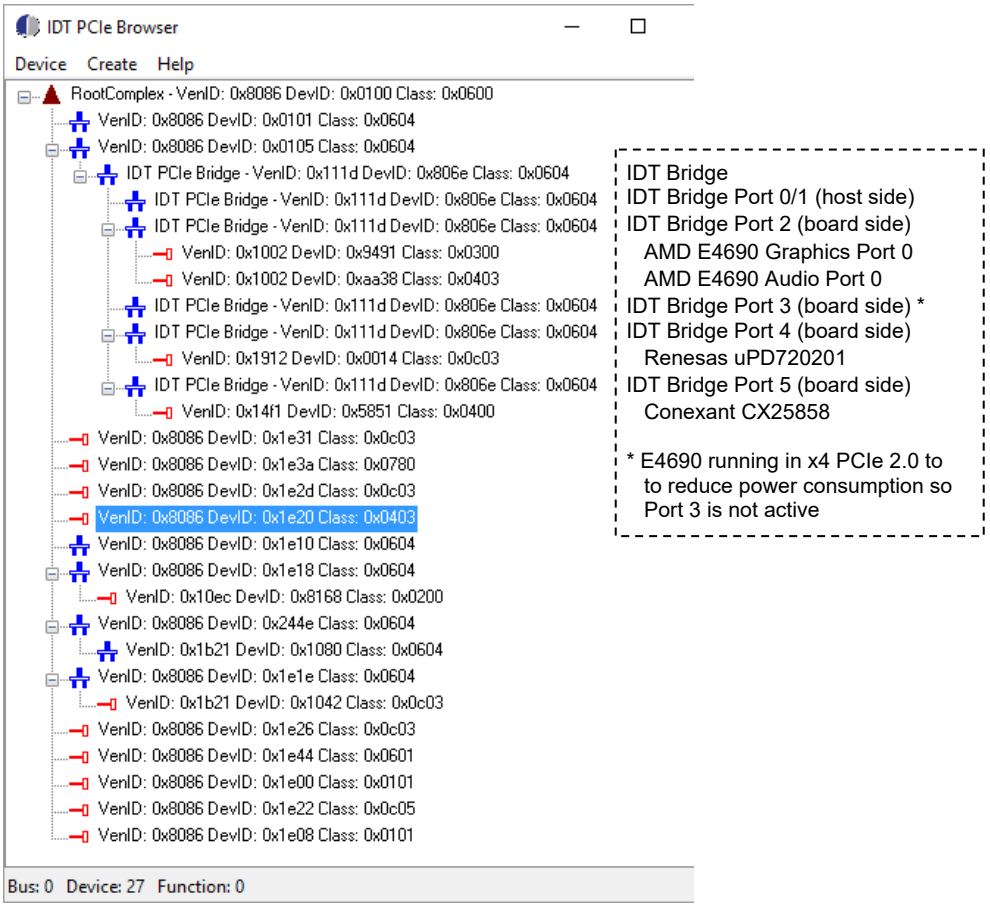
8.2 IDT 89HPES24T6G2 PCIe Switch

All operating systems should deal with the switch correctly and its operation should be completely transparent.

One nice piece of Windows software that can be very handy is IDT's PCIe Browser. With it, you can scan all the PCIe links and see all devices that are connected. A current link for the PCIe Browser is:

IDT PCIe Browser

Figure 8-1 Sample IDT PCIe Browser Screen Shot

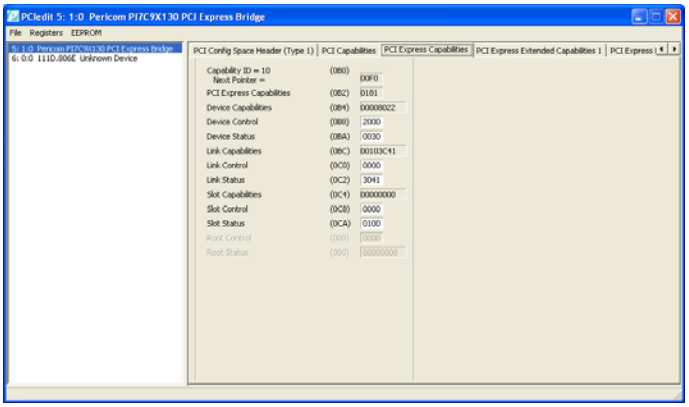


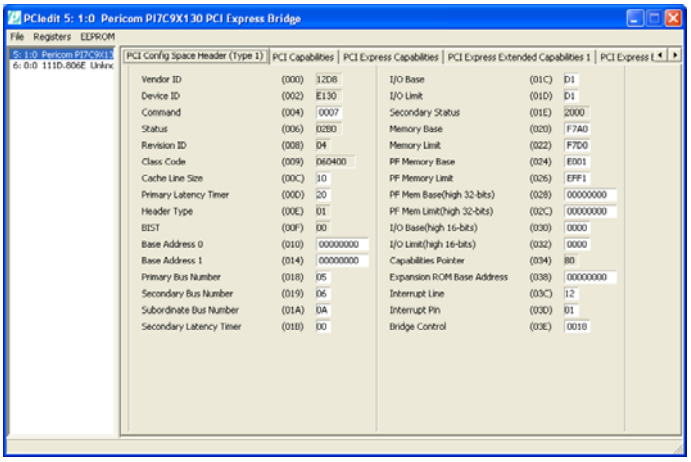
8.3 Pericom PI7C9X130 Bridge (AgatePXC, MerlinPXC)

The Pericom PI7C9X130 is a PCIe x4 to PCI 32/64 PCI bridge and is active when the AgatePXC or MerlinPXC is installed. Note this does not include the MerlinMTX, which has no PCI interface. As with the IDT PCIe switch, all operating systems should deal with the 9X130 correctly and its operation should be completely transparent.

Pericom supplies a program called PCIedit that works on W10. There are 32-bit and 64-bit versions available. Here are a couple of sample screens.

Figure 8-2 Sample Pericom PCIedit Screen Shots





In both screens, the Unknown Device is actually the IDT PCIe switch that is connected to the PCIe side of the 9X130 and which provides access to all of the Agate or Merlin onboard devices. See the AgatePXC, MerlinPXC, and Merlin MTX block diagrams in Chapter 1.

8.4 Renesas uPD720201 USB Controller (AgatePXC, MerlinPXC)

With the advent of Windows 10, drivers for the Renesas uPD720201 are finally included in the OS itself. However, for XP, Vista, and Windows 7-8.1, you have to install drivers. Renesas does not supply drivers directly.

There is no driver distribution for Linux. According to Ubuntu, you just need to run a Linux kernel of not earlier than 4.4.

You can obtain a suitable Windows 7-64 driver:

uPD720201 Drivers for Windows

Scroll down the window and you should find a Download link. Save the file to c:\temp. You should have something like this:

c:\temp\renesas_usb_3.0.23.0(www.station-drivers.com).exe

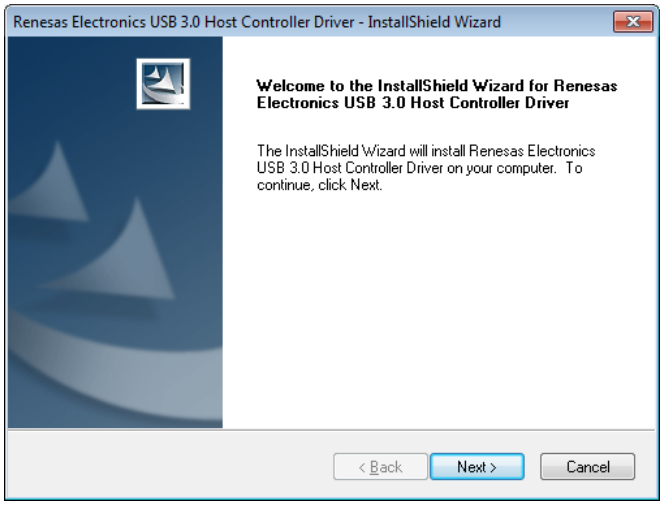
Double click on it and the installer will unpack the files. Run the setup exe:

c:\temp\[directory]\RENESAS-USB3-Host-Driver-30230-setup.exe

and then you find more files. Enter:

c:\temp\[directory]\USB3-201-202-DR-WIN-20120531\EXE

Figure 8-3 Renesas Example Installation Screen Shot



Once it is done running and Windows is done thinking, you can go to Device Manager, look in USB devices, and see that the uPD720201 is installed. See Figure 7-14 in Section 7.9.

8.5 AMD E4690 Graphics Controller (AgatePXC)

AMD supplies graphics drivers for the E4690. However, in its infinite wisdom, AMD has chosen not to support graphics drivers for the E4690 beyond Windows 7.

Windows 8-10 uses the Microsoft Basic Display Driver even though Device Manager Properties tab claims that the driver is an AMD driver.. This would not be a big deal except that you can't get a screen resolution better than 1600x1200, and worse yet, there is support for only one screen.

You can still install an AMD E4690 driver but the OS won't actually use it, even if Device Manager shows that you have an E4690 installed. Just look at the Driver Details tab and it will say that no driver is installed.

It's also not possible to force-install the driver on Windows 10 because when you do (by double-clicking on c:\8.961-120405a-137848C-EDG_Direct\Packages\Drivers\Display\W76\ CH137848.msi) W10 says the driver is for Vista and refuses to install it.

If you look in the AMD-supplied-to-Windows 10 install tree at c:\Windows\System32\DriverStore\FileRepository\c0313676.inf_amd64_96bbc33bec5c7fae\c0313676.inf, the file has "%AMD9491.1%" = ati2mtag_Legacy, PCI\VEN_1002&DEV_9491

If you have a developer setup, know what you are doing, and can re-sign drivers (which we can't), the %ATI% = ATI.Mfg, NTamd64.6.0, NTamd64.6.1 line in the inf file has to be changed and, more as well. But, we don't know what that is. There is more to it because changing the Mfg line to include NTamd64.6.3 didn't make a difference.

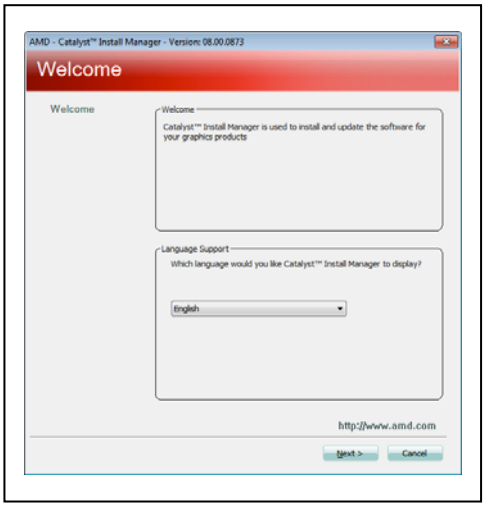
8.5.1 E4690 Windows Driver

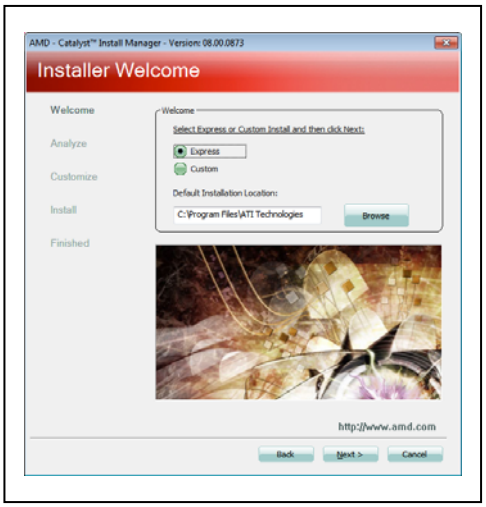
If you have W7 or earlier, retrieve the AMD Legacy Embedded GPU and Chipset Vista/Win7 Driver.

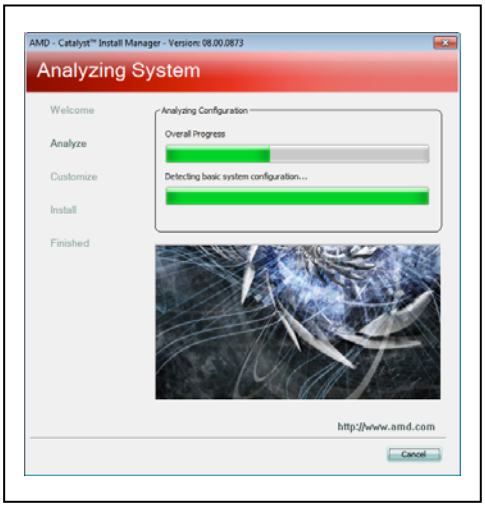
8.5.2 E4690 Linux Driver

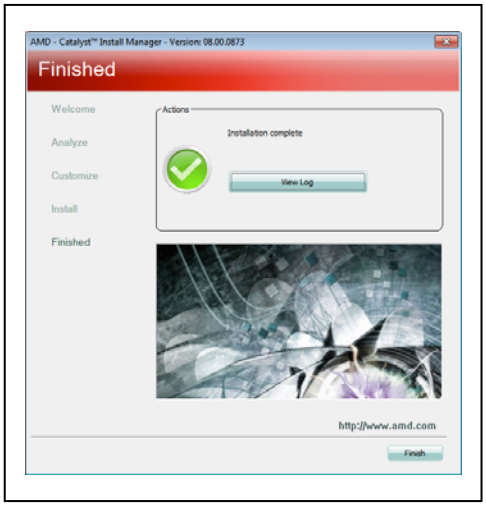
For Linux, retrieve AMD Catalyst 12.4 Proprietary Linux x86 and x86_64 Display Driver for X.Org 6.7 -7.6.

Figure 8-4 Sample AMD Catalyst E4690 W7 Install Screen Shots









8.6 AMD E8860 Graphics Controller (Merlin)

AMD supplies graphics drivers for the E8860 with support including Windows XP, 7, 8, and 10.

For XP, please contact Rastergraf.

To get the latest versions for Windows 7, 8, or 10, go to:

http://support.amd.com/en-us/download

Then, under Manually Select Your Driver,

Step 1: Embedded Graphics

Step 2: Radeon Embedded

Step 3: E8860

Step 4: Windows version (choices include 7, 8, and 10, 32/64 bit)

AMD Catalyst Windows 64-bit Display Driver for Windows 10 64-bit and Windows 7 64-bit.

Download the file to your C:\Temp directory or if the download puts the file in your Downloads directory, move it to C:\temp. Installs may not run out of Download. The file will look something like this:

C:\temp\16.60.2601-170214a-312166c-aes.zip

Then, unpack

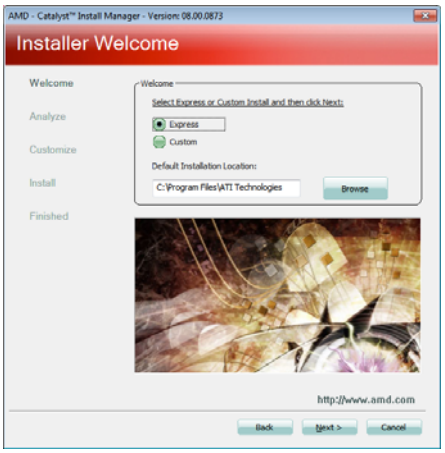
Locate the setup file and double click on it to start the setup.

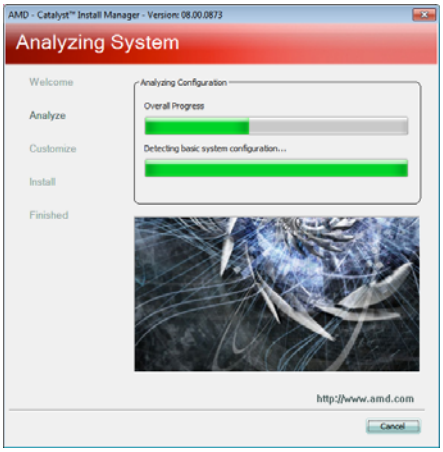
When running this install, just double-click on the .exe file and wait. After the install completes. You should wait a little while for Windows to realize that the driver is installed, and you may get some message.

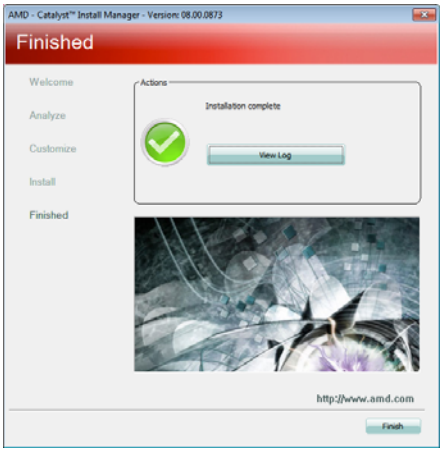
You should reboot once everything is settled down and BEFORE doing anything else. Don't do any other installs until after you have rebooted.

After you are back up and running, you may need to adjust the screen resolution(s), but usually, the driver sets things up the way they should be.

Figure 8-5 Sample AMD Catalyst Typical Install Screen Shots







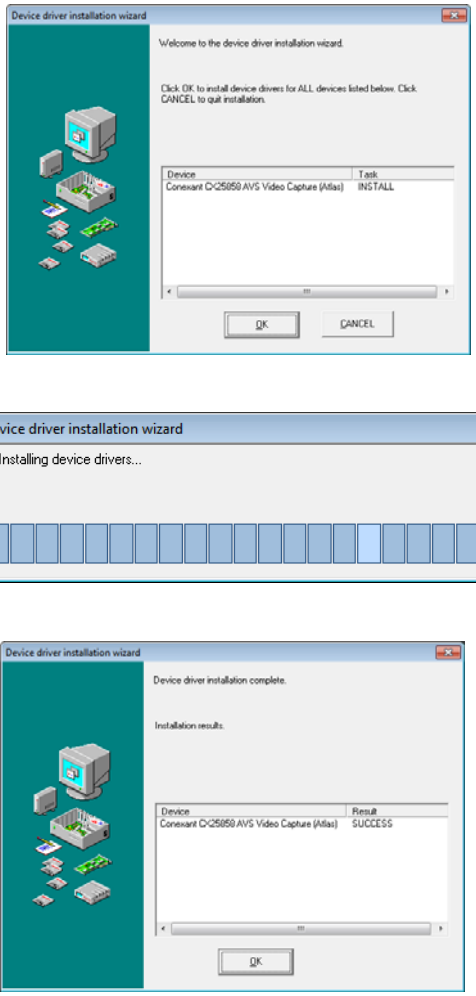
8.7 Conexant CX25858 Digitizer (AgatePXC, MerlinMTX)

The software can be obtained from Rastergraf. Install as follows:

C:\temp\AtlasWin64_7.0.118.64\Conexant\Atlas_x64\fre\Setup64.exe

A popup will ask you if you want to install the driver. Select the line that shows the CX25858 and say OK. The installer should also have installed CxHelios, which is a simple demo program. Note that CxHelios will ONLY run on PCIe-based system.

Figure 8-6 Conexant CX25858 Install Screen Shots



One side note: Section 8.8.4 describes couple of programs that do enumerate the CX25858 but only sort of work with it. You can select the CX25858 as a device for viewing on AMCap or e-CAMView, but we have gotten only a flickering image on AMCap and nothing at all on eCAMView.

8.8 Cypress FX3/CX3 (AgatePXC, MerlinPXC)

8.8.1 Installation

8.8.1.1 Introduction

In order to access the Cypress CX3 (AgatePXC, Merlin PXC) or FX3 (Agate only) you have to install the Cypress EZ-USB FX3 Software Development Kit. While there are some CX3-specific app notes and code, there is no CX3-specific SDK. You have to download the FX3 SDK, which supports the FX3, CX3, and other devices in the family. The FX3 SDK is available for Windows, Linux and MacOS.

The current version of the SDK supports the FX3 and CX3. The CX3 devices provide a MIPI CSI interface that can connect directly to image sensors. The FX3 SDK is available for Windows, Linux and MacOS.

8.8.1.2 EZ-USB FX3 SDK Installer

This is the master installer file that will install the firmware library with samples, USB Suite with Windows host driver and applications, Eclipse IDE & GCC tool chain. Once installed using the installer, Cypress Update Manager will monitor Cypress for updates and facilitate upgrades.

8.8.1.3 Firmware Library Zip

A zip archive that contains the FX3 and CX3 firmware libraries, complete FX3 and CX3 firmware sources, header files, example code, firmware conversion utility, documentation, and many firmware source samples.

8.8.1.4 USB Suite Zip

A zip archive containing windows host driver, C++ & C# API libraries, and the control center, bulkloop and streamer applications for 32-bit platforms (Windows XP/7/8/8.1) and 64-bit platforms (Windows 7/8/8.1).

NOTE: as it comes from Cypress, the current version of the SDK (1.3.3) does not support Windows 10. A separate driver distribution is available here: Cypress 32/64 bit drivers up through W10.

8.8.1.5 USB Suite Source Code Zip

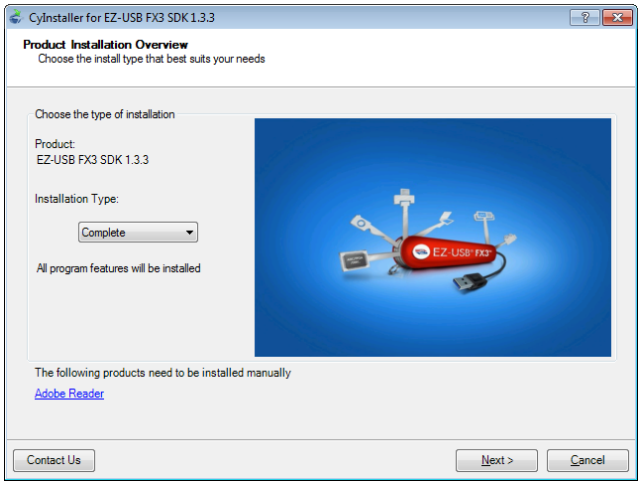
A zip archive containing windows host driver source code and the C++ & C# API library source code

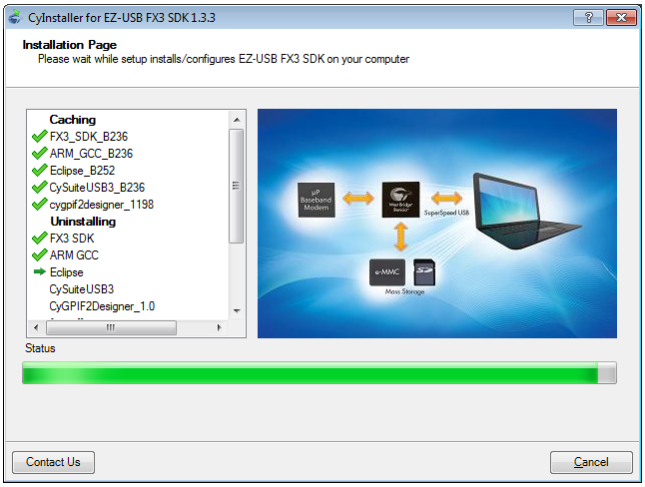
8.8.1.6 Documentation

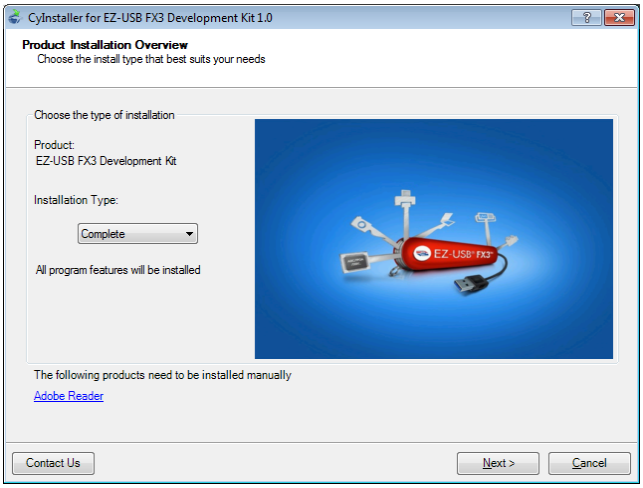
FX3 Programmer's Manual, API guide, SDK Release Notes, and SDK Trouble shooting guide; USB Suite Release Notes and Quick Start Guide.

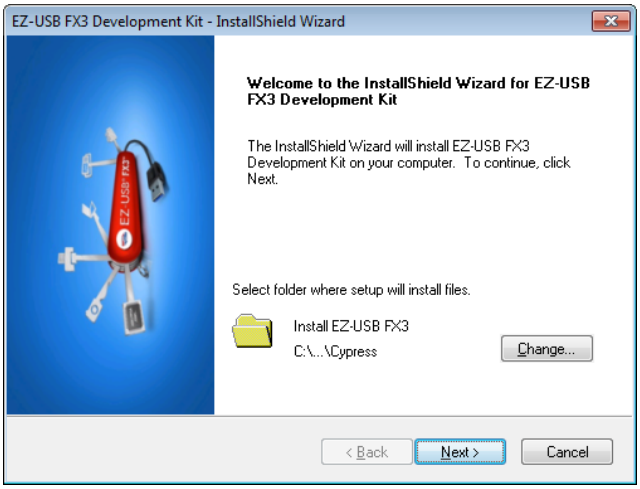
Please be sure to go on to Section 8.8.2, Driver Notes.

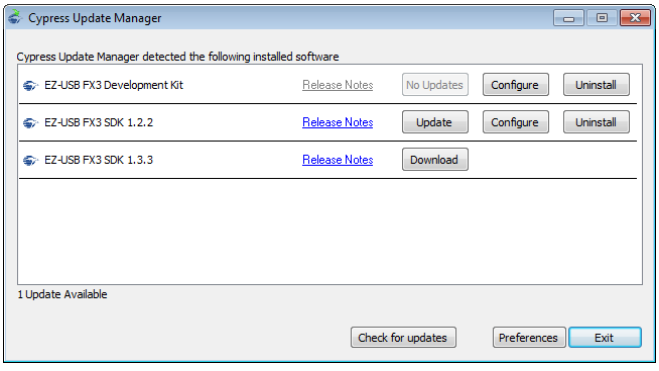
Figure 8-7 Cypress Example Installation Screen Shots











8.8.2 Driver Notes

8.8.2.1 Introduction

The Cypress FX3 (Agate only) and CX3 (Agate, MerlinPXC) are USB SuperSpeed devices which are connected to the on-board Renesas uPD720201 controller. In order to use them:

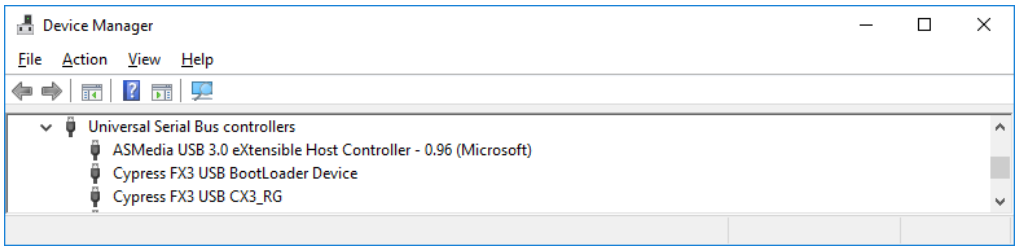
a) the Renesas uPD720201 USB driver must be installed for XP-W7 – see Section 8.4. On W10, the driver is built-in;

b) the Cypress SDK software must be installed – see Section 8.8.1;

c) For W10, the Cypress 32/64 bit drivers up through W10 must be installed because SDK Version 1.3.3 does not support Windows 10.

Having done all that, go to Device Manager and you should see the two Cypress lines shown in the figure below for AgatePXC. For MerlinPXC, only the CX3_RG line will appear.

Figure 8-8 Device Manager Screen Shot Showing Device Presence



Unless you can see this, you will not be able to proceed further.

8.8.2.2 Reprogramming the SPI PROM

You may wish to write your own software for the CX3 or FX3 and burn it into the SPI PROM instead of running it in RAM. We don't recommend this because having the default "Blinker" program in SPI PROM is a good way to tell that the CX3 or FX3 is working. In any case, it is easy to recover and program in a known-good image. See Section 7.10.1.

8.8.2.3 Caution About Driver Vendor and Product ID Codes

When writing your own software you want to identify the code by including a new Device ID in the driver inf file (cyusb3.inf) – see page 8 of the Cypress CyUsb3.sys Programmer's Reference for details.

This works up through W7 because the OS did not require the driver to be signed and did not enforce hash coding. Alas, W10 does all that and more. You can't touch the inf file unless you can sign the driver and have an EV SSL certificate. So, if you do want to use a different ID, pick one that is already in the inf file and that you know will not be used by your users. There are a LOT to choose from. See Section 2.6.4 for more information

8.8.3 Installing a driver that Windows 10 doesn't like

It can happen that you want to install an older driver that isn't signed and/or doesn't have an accurate hash code.

Starting in W8, drivers are required to be have a digital signature. Thus, in W8/8.1/10, if you try to use an XP or W7 driver that may be perfectly good, the OS will typically give you a message like this:

The hash for the file is not present in the specified catalog file. The file is likely corrupt or the victim of tampering.

In order to install that XP or W7 driver, you have to temporarily "disable driver signature enforcement".

Here is a link that has a really good procedure:

http://www.dinolite.us/support/using-older-models-with-windows-8-10

Having done this procedure, you should be able to use an XP or W7 driver on W10.

8.8.4 Useful CX3 Programs

The following programs have been tested with the WandCAM. Both programs can be a little fragile (or maybe its DirectShow that's fragile). It's not recommended to tinker with any of the default settings. If the program does hang, you usually have to reboot the system to recover.

8.8.4.1 AMCap

AMCap is a simple Windows DirectShow tool that lets you capture video from your webcam. With AMCap you can easily record video to your hard drive, either in MPEG2 or AVI format, provided you have the necessary codecs. It features some other interesting options, such as the ability to take screenshots or adding special effects to the image (graphic overlay, alpha-blending, transparency, etc.).

The website that has AMCap also has several other useful programs.

8.8.4.2 e-CAMView

e-CAMView is a Windows DirectShow camera application for video streaming and still capturing from the USB camera device. e-CAMView comes with a set of features that can be used to attain the full functionality of the USB cameras. All the connected DirectShow video & audio devices are listed in an e-CAMView menu. Just choose one and start streaming. e-CAMView displays the resolution and the frame rate in a status bar.

8.9 ST Micro STM32F427

There are several aspects to the host system software required to access the Integrated System Monitor (ISM) firmware that Rastergraf has loaded into the STM32F427 flash memory:

There is the USB Port Side Driver, a host-based terminal emulator, and SWD-DP firmware update software as well as optional components that use the DFU mode and the Discovery development board. These are covered in the subsections that follow.

To learn more about ISM, please refer to Section 1.10 for more about the ISM. Please refer to Section 6.3 for information about how to use the ISM.

Please note that you will need to have administrator privileges to successfully install some of the software mentioned in these sections.

8.9.1 USB Host Side Port Driver

In order to communicate with the Merlin ISM code, you have to first install the ST Micro USB host port driver. This software enables the ISM to communicate with a terminal emulator program via a host COM port.

In order to install the ST Micro USB Driver, follow this procedure:

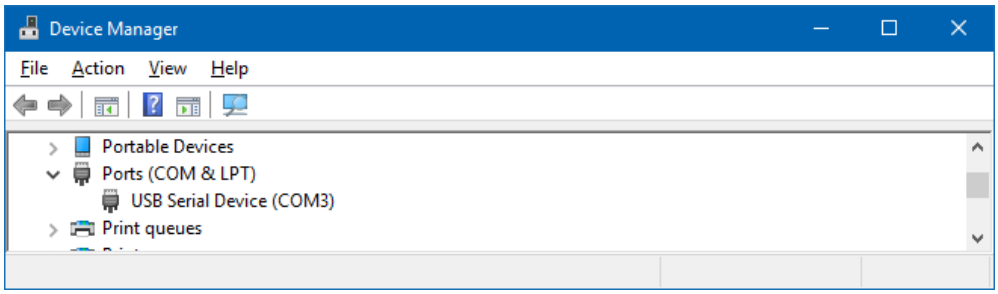
a) download STSW-LINK009 into your c:\temp directory

b) extract the files to c:\temp\en.stsw-link009.

c) run c:\temp\en.stsw-link009\ dpinst_amd64.exe for 64-bit OS or
run c:\temp\en.stsw-link009\ dpinst_x86.exe for 32-bit OS.
Don't worry about the file names – they both work on AMD and Intel.

d) Please refer to Section 3.7.2 for connecting to the Mini B port.

Now, once the Merlin is powered up and you plug the Merlin Mini-B connector into a host port, you will get a couple of messages that the port is being set up and you should see something like this in Device Manager:



And, if you unplug the Merlin, this port will disappear.

8.9.2 Terminal Emulator

In order to communicate with the ISM software on the Merlin or the ST Micro Discovery board, you need to have a terminal emulator program running on your host system. Two common ones are PuTTY and HyperTerminal.

8.9.2.1 PuTTY

A modern comm program that does a lot more than just terminal emulation is PuTTY. There is a 32-bit version and a 64-bit version as well as Unix versions. PuTTY is a client program for the SSH, Telnet and Rlogin network protocols. It also can support Raw and Serial connections.

These protocols are used to run a remote session on a computer over a network. PuTTY implements the client end of that session: the end at which the session is displayed, rather than the end at which it runs.

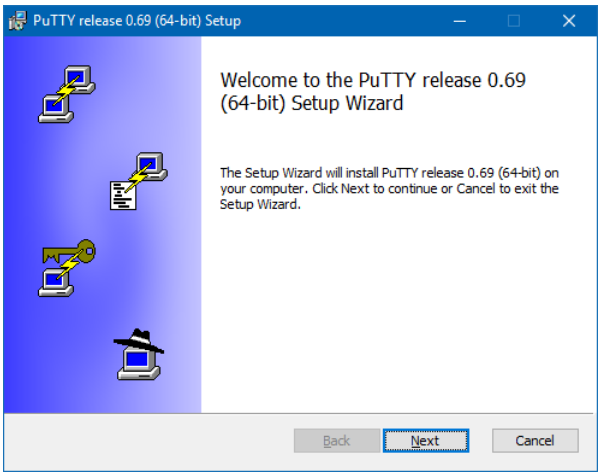
In really simple terms: you run PuTTY on a Windows machine, and tell it to connect to (for example) a Unix machine. PuTTY opens a window. Then, anything you type into that window is sent straight to the Unix machine, and everything the Unix machine sends back is displayed in the window. So you can work on the Unix machine as if you were sitting at its console, while actually sitting somewhere else.

In order to use PuTTY, the **Merlin must be powered up, the Merlin Mini B connector must be linked to a host USB port, and the ST serial driver has been installed**. Then, in PuTTY, you select Serial mode and the COM port (in our example, COM3) and it should just work.

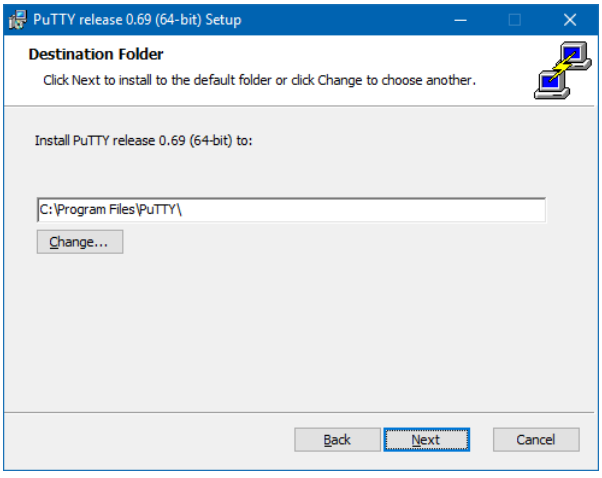
To install, download the PuTTY distribution and put it in your c:\temp directory. The 32-bit file name is putty-0.69-installer.msi. The 64-bit file name is putty-64bit-0.69-installer.msi.

Double click on the .msi and you will get:

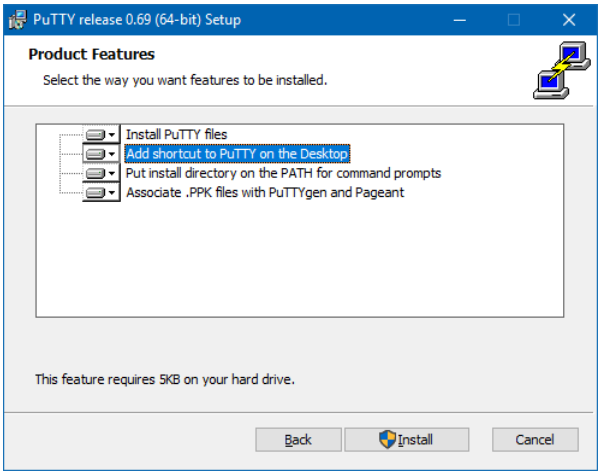
Screen 1



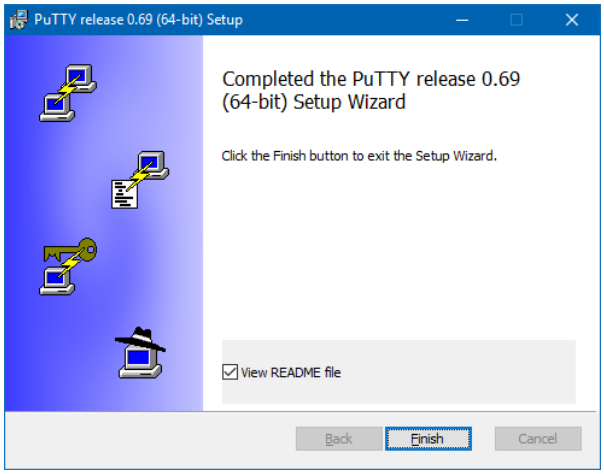
Screen 2



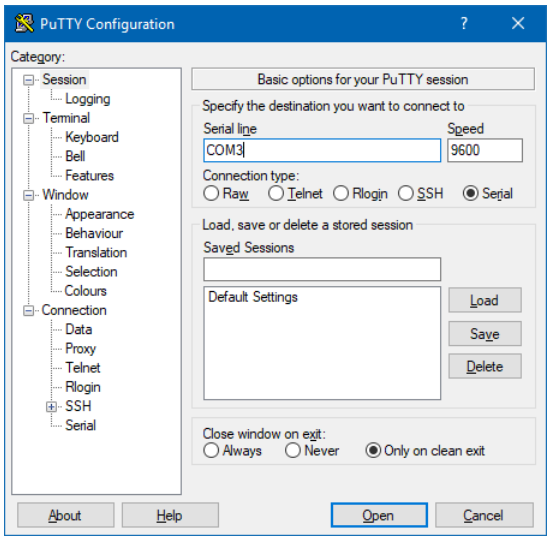
Screen 3



Screen 4



Screen 5



Screen 6

Note that the default screen has white characters on a black screen. To get the Screen 6 settings, go to Window > Colours, change the Default Foreground to, say, 75/75/75, Default Background to 255/255/255, Cursor Colour to 0/0/0 and then go to Window > Appearance, and change the cursor to underline.

8.9.2.2 HyperTerminal

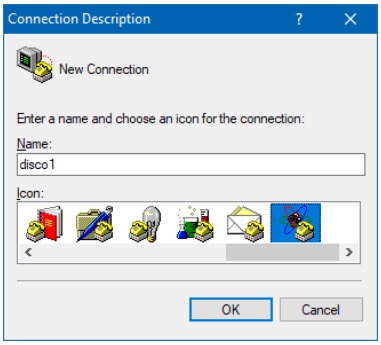
The tried and true terminal emulator for Windows has always been HyperTerminal. But, as of Windows 7, Microsoft stopped distributing it.

However, HyperTerminal does run on W7 or W10. And, if you have an XP system still running, you can extract three files from your XP installation and copy them over to Windows 7 or W10:

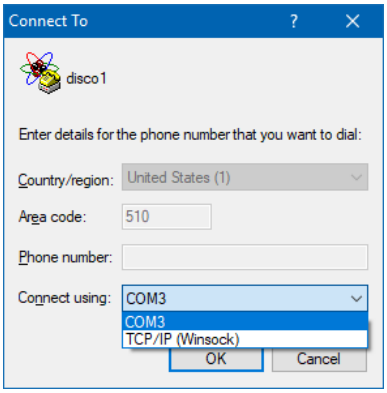
hypertrm.exe, hypertrm.dll, and hticons.dll.

Create a directory c:\program files (x86)\hyperterminal and put the files in there. Create a shortcut to hypertrm.exe on your Desktop. It should just work

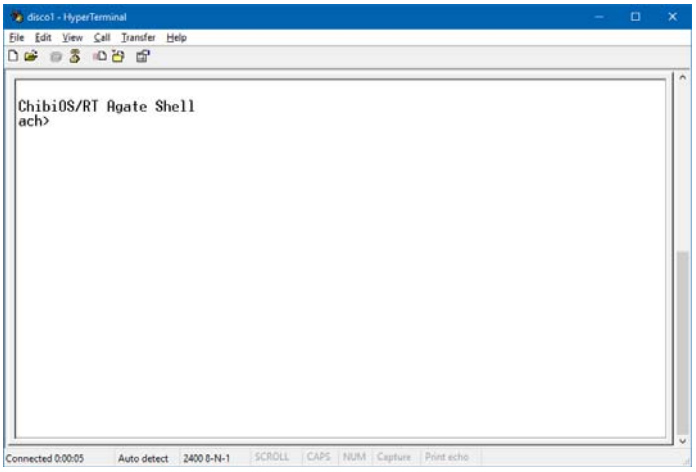
When you first run it, you will get a popup about creating a modem. Say yes, and you shouldn't get the message again. Then, you will get a popup:



Type a name into the Name box (like disco1), and you can pick an icon from those shown. The next popup will give you port to select. **If you have the Merlin powered up and running and the Device Manager shows that the COM port is active** (see previous page), then you should see that COM port show up in the Connect using:, as shown in this figure.



Once you say OK, you should get a popup:



The message will differ depending on the board and ISM firmware version. The screen shown here is for an older version of the firmware..

When you exit, you will be asked if you want to save the file (if you didn't save it before). If you say yes, then the next time when you start up HyperTerminal, just close the new connection popup and go to File > Open and find the file that you saved.

8.9.3 SWD-DP Debugger Port

The SWD-DP port on the STM32F427 is used to update the firmware that is flashed into the chip. You can access this port on the Merlin via the Micro AB connector located near the from panel.

If you would prefer to have Rastergraf do a firmware update, obtain an RMA # from us and we will do the update at no charge except shipping.

THIS IS NOT A USB COMPATIBLE PORT. DO NOT CONNECT THIS PORT TO ANY USB PORT OR YOU MAY DAMAGE THE STM32F427.

WE USE A USB CONNECTOR AND CABLE BECAUSE IT MAKE CABLING EASIER.

In order to use the port, you have to order an ST-LINK/V2 from Digikey or Mouser. It provides the interface between a host USB port and the STM32F427 SWD-DP port.

You also have to build a cable to connect the ST-LINK/V2 to the Merlin Micro AB connector. Please refer to Section 3.7.1 for information about building the cable. Rastergraf can supply a cable for a nominal charge.

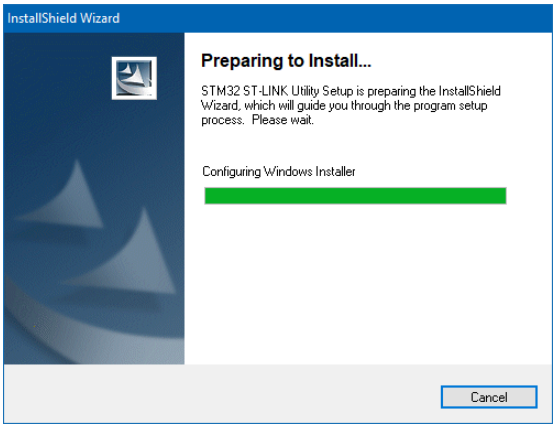
You will need to install the ST-LINK/V2 software: STSW-LINK004. Optionally, you can also install the ST-LINK/V2 firmware update: STSW-LINK007.

In order to install the ST-LINK/V2 software, follow this procedure:

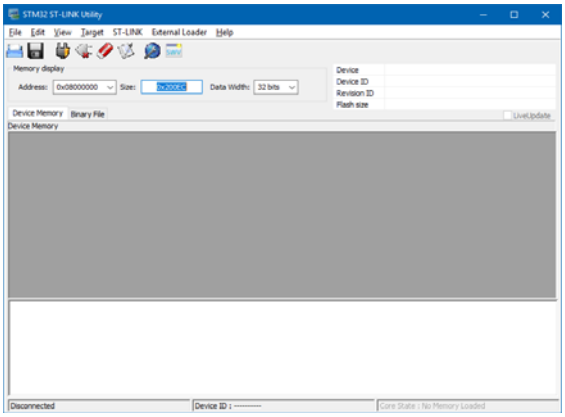
a) download STSW-LINK004 software into your c:\temp directory:.

b) Extract the files into c:\temp\en.stsw-link004.

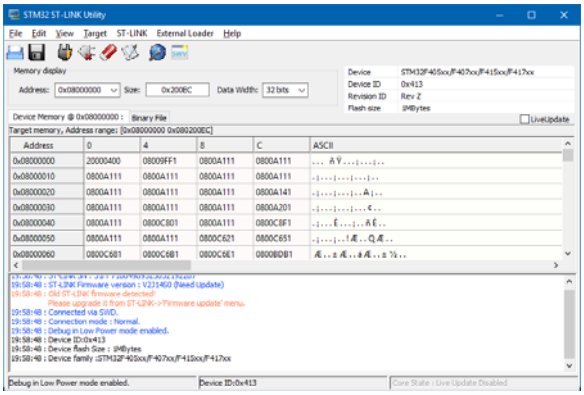
c) run c:\temp\en.stsw-link004\STM32 ST-LINK Utility v4.0.0 setup.exe



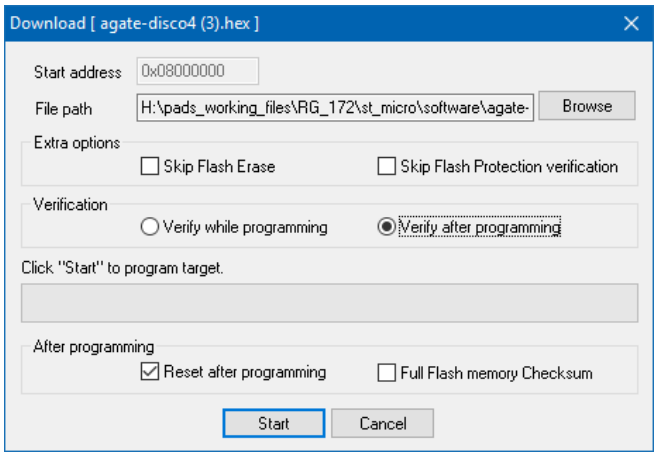
Ensure that the Merlin is powered up, the STLINK/V2 USB cable is connected to a host port, and the Merlin AB to STLINK/V2 20-pin header cable is installed. Start the STM32 ST-LINK Utility and get this screen:



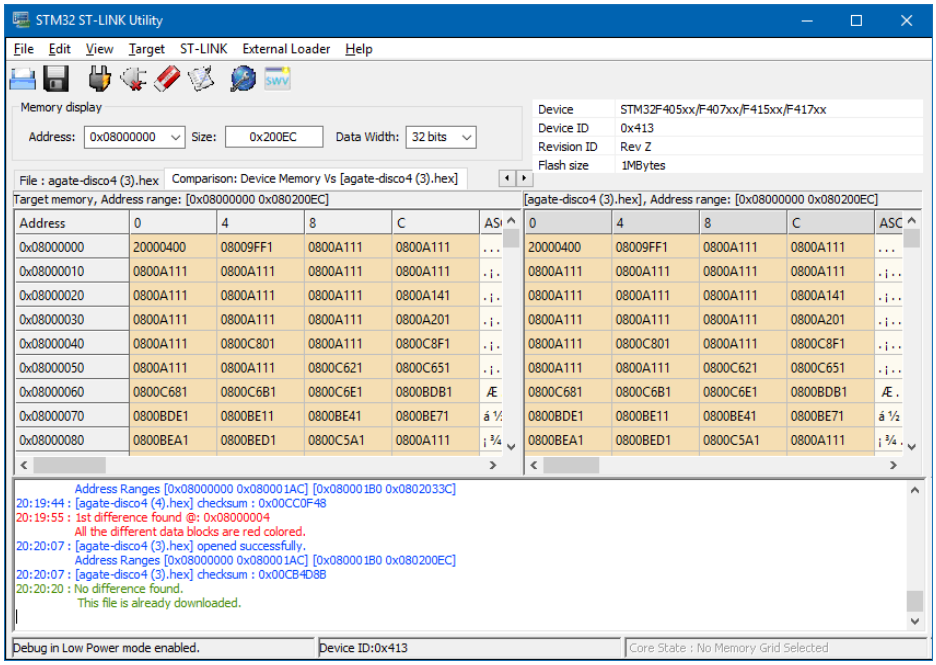
Now, go to Target > Connect. If your computer sound is turned on you will hear a little tune and the screen will change to this screen:



Now, you can open a new firmware file and then enter <CTRL-P>, which will initiate the reprogram process. We recommend that you change the Verification option to Verify after programming



Alternatively, you could verify flash image. Open up the file to be compared and then under Target, select Compare device memory with [file name]. This screen shows a successful comparison.



8.9.4 DfuSe USB device firmware upgrade

The ST Micro ARM devices like the STM32F427VI that is used on the Merlin have an alternate way of downloading software into memory called Device Firmware Update (DFU). It allows a new firmware image to be loaded into a selected part of ST memory via the FS USB port of the ST chip. This can be used if, for instance, you don't have access to the SWD-DP port, or if you want to download an image into another part of memory without affecting the primary image.

You can read more about the DFU here and here.

There is a DFU demo program that can be installed and is interesting to tinker with. You have to put the Merlin into DFU mode to use it. The software is the DfuSe USB device firmware upgrade STMicroelectronics extension: STSW-STM32080

It is beyond the scope of this manual to go any further into DFU.

8.9.5 ST Micro STM32F4DISCOVERY Demo Board

ST Micro makes a variety of demo boards for its CPUs. While there isn't a specific board for the STM32F427VI that is used on the Merlin, there is one for the STM32F407, which is a very close relative. This document, starting on page 3, provides a detailed comparison between the devices.

Except for some bug fixes in the '427, the most important difference from the Merlin's perspective is that the flash size is 2MB instead of the '407's 1MB. But, the ISM code doesn't come close to exceeding 1MB at this point.

It may be handy to have one of these boards around to tinker with, especially if you are thinking of writing your own code for the Merlin board. The board is called the STM32F4DISCOVERY. Go to the page at that link and you will find lots of documentation as well as a link to the development software. It only costs about $20.

You can order the STM32F4DISCOVERY board (order code **STM32F407G-DISC1)** from Digikey or Mouser.

8.10 Installation Procedure for Windows

This section suggests a procedure for installing the software necessary to use an Agate or Merlin graphics board on Windows Systems.

It is assumed that a XP system will be 32-bit and W7 – W10 will be 64 bit. It does make a difference for many drivers.

One difficulty in doing this is that the graphics board is essential for the use of virtually all Windows-based systems. Unless you are using a serial terminal console, you need a graphics board to use the OS.

There are two possible scenarios to consider:

a) you are building a new system and the Rastergraf board is included as part of the system integration project;

b) you are adding the Rastergraf board to an existing system. The current graphics card will be disabled or the BIOS will be set to prefer the Rastergraf board upon booting.

In either case, you have to see that the Rastergraf board at least gives you boot-up screens and allows you to log into Windows before you can do anything else. Chapter 5 covers all of the mechanical aspects of installation, so you should have looked at that already.

Assuming that you have been able to log into Windows and have a satisfactory display using the Rastergraf board, you can now proceed to the software installation. Please refer to previous sections of this chapter for source web sites for the necessary software.

You may notice that once you are logged in that you will get some popups saying that Windows is installing, or wants to install software for the devices it has found on the Rastergraf board. Just ignore or cancel the popups, they will get taken care of in the installation procedure that follows.

In all cases, when running an install, don't do anything else on the computer. You may miss a query or otherwise mess things up. Just be patient.

Step 1: Agate/Merlin (all) - Install the Graphics Driver

For Agate, see Section 8.5 for the file location.

For Merlin, see Section 8.6 for the file location. For Merlin XP, please contact Rastergraf for the correct image. It is not available on the public AMD web site.

When running this install, just double-click on the .exe file and wait. After the install completes, you will need to reboot before doing anything else. **Don't do any other installs** until after you have rebooted.

After you are back up and running, you may need to adjust the screen resolution(s), but usually, the driver sets things up the way they should be.

Step 2: AgatePXC/MerlinMTX - Install the Conexant Driver

Following the appropriate link provided in Section 8.7, install the Conexant CX25858 driver. A popup will ask you if you want to install the driver. Just select the line that shoes the CX2585 and say yes. The popup will refresh when it is done and say that it was successful. You can close the popup and proceed to the next step.

Step 3: AgatePXC/MerlinPXC - Install the Cypress SDK

Following the appropriate link provided in Section 8.8, install the Cypress SDK. We advise selecting the complete install.

Once the installer has finished, it will show a popup with the update manager. If there is a newer version, it will offer to download and install that for you. You might as well allow it to do that. If the updater doesn't have an active button for any downloads, then just exit.

You may need to reboot at this point.

Step 4: MerlinPXC - Install the USB Driver – All but Windows 10

Following the appropriate link provided in Section 8.4, install the Renesas uPD720201 driver.

Once you have installed the USB driver, you will get new Windows installer popups telling you that it is installing software for new devices – theses are the FX3 and CX3 that are connected to the USB controller. These should proceed automatically and eventually you will get messages saying that they have been completed.

You may want to reboot at this time.

OK, you are done with all of the necessary installations for Windows.

8.11 Installation Procedure for Linux

To be added

Chapter 9
Notes for AgatePXC Rev 0&1

9.1 Introduction

This section covers the unique features of the AgatePXC Rev 0 and Rev 1, of which only a few each were built:

9.1.1 Revision 0

Major revisions of Rev 0 became necessary due to the loss of particular function that AMD chose not to support in the E4690 graphics controller.

Also, the processor that provides the on-board In System Monitor was changed from a Microchip PIC18F47J53 to the ST Micro STM32F427 due to a number of limitations in the chip that were not apparent during the initial design. In addition, some changes were made to the power control circuits.

One significant layout error in the CX25828 subsection was corrected. In Rev 0, the audio and video inputs components were inadvertently swapped. The result was that the A/V pinout section of the Honda SDR50 connector was incorrect and a number of components were mis-specified.

With respect to this error. it is possible to easily transition from the Rev 0 to the Rev 1 in all respects EXCEPT that the Honda SDR50 connections will be different.

9.1.2 Revision 1

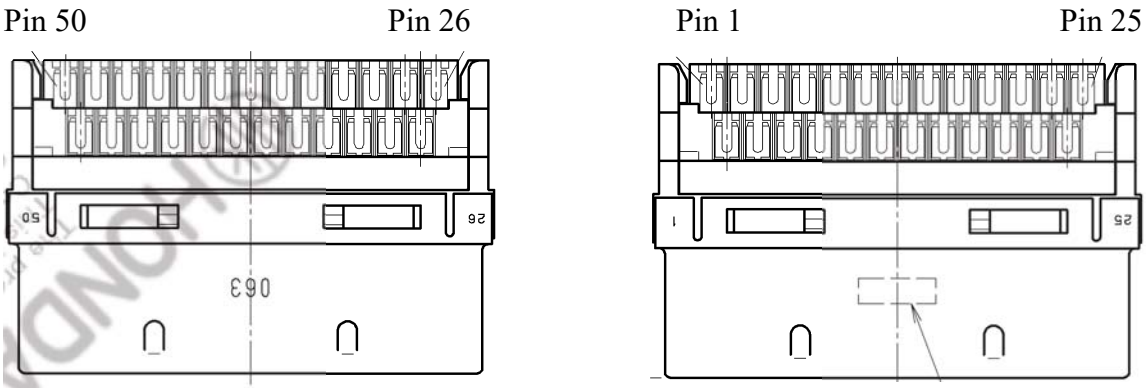
Note that Agate Rev 1 uses a Mini AB connector which is a bit taller than the Micro AB. You need to be careful about clearance between adjacent boards and the connector

9.2 Multi-Function I/O Connector (AgatePXC/2 Rev 1)

The AgatePXC/2 has a front panel Honda SDR50 (HDR-EC50LFDT+) I/O connector that supports 2 different pinout option: 50A and 50B. The latter is available only by special order.

Figure 9-1 Typical SDR50 Connector

Mating connector: HDR-E50MSG1+ and HDR-E50LPH shell - see onlinecomponents



Cable sets follow connector pin arrangement: twisted wire pair plus ground. Use this arrangement to get even length of wire pairs through the connector

9.2.1 SDR50 Pinout: DVI In, RGB In, USB 3.0, 8x Audio/Video In

This includes a 8 NTSC/PAL video inputs, 8 audio inputs, an RGBHV input, a DVI input, and a USB 3.0 port.

If you look ahead to the Pinout Table, you will see that the pins are listed according to their intended grounds. If you plan to build your own cable, please follow this arrangement.

9.2.1.1 8x NTSC/PAL Inputs

VIN1-VIN8 are composite NTSC/PAL Inputs. Each input is connected to the CX25858 digitizer by a 1.0 uF input capacitor and presents a (DC) 75Ω impedance to the driving source. No low pass filtering is done on the signals. Each VINx has its own A to D converter and DMA transfer engine, which allows all 8 channels to be acquired at the same time. The cabling should use 75Ω coax.

9.2.1.2 8x Audio Inputs

AIN1-AIN8 are audio inputs configured as four stereo pairs..

The inputs are connected to the CX25858 digitizer by a 2.2 uF input capacitor and present a high impedance of about 180KΩ at 500Hz to the driving source. No low pass filtering is done. They each have their own A to D converter and DMA transfer engine, which allows both channels to be acquired at one time. The cabling should use 50Ω coax.

9.2.1.3 DVI and RGBHV Inputs (non-functional)

The I/O connector can be used to connect to the high-speed RGBHV or DVI inputs of the ADV7441A to acquire DVI, RGBHV or RGB + SOG, up to 1600 x 1200 at 160 MHz.

The RGB inputs are connected through front-end Murata NFL21SP107 100 MHz low-pass filters and then to the ADV7441A by a 0.1 uF input capacitor. They present a (DC) 75Ω impedance to the driving source. The cabling should use 75Ω coax.

The output of the ADV7441A is linked to the E4690 input port and because AMD has decided not to support this function, neither the DVI nor RGBHV input capability can be used.

9.2.1.4 USB 3.0 Port

The Agate MIPI port supports a USB 3.0 on the SDR50 connector. The matching cabling must be done very carefully as the SSRX and SSTX pairs must be matched length pairs and don't work well if they aren't. Testing of this port shown that while USB 2.0 mode works fine, the USB 3.0 mode is a bit unreliable and thus, you might not want to try to use it.

Table 9-1 Multi-function I/O Connector (AgatePXC/2 Rev 0)

SDR Pin	Standard Pinout	SDR Pin	Standard Pinout
1	GND	26	FP_USB_SSTXP
2	FP_DVI_IN_CN	27	FP_USB_SSTXN
3	FP_DVI_IN_CP	28	FP_USB_V
4	FP_DVI_IN_2N	29	FP_USB_SSRXP
5	FP_DVI_IN_2P	30	FP_USB_SSRXN
6	FP_DVI_IN_1N	31	GND
7	FP_DVI_IN_1P	32	FP_USB_DP
8	FP_DVI_IN_0N	33	FP_USB_DN
9	FP_DVI_IN_0P	34	GND
10	GND	35	FP_R_IN
11	FP_VS_IN	36	FP_G_IN
12	GND	37	FP_B_IN
13	FP_HS_C_IN	38	GND
14	GND	39	GND
15	FP_VIN6	40	FP_VIN8
16	FP_VIN5	41	FP_VIN7
17	GND	42	GND
18	FP_VIN2	43	FP_VIN4
19	FP_VIN1	44	FP_VIN3
20	GND	45	GND
21	FP_AIN6	46	FP_AIN8
22	FP_AIN5	47	FP_AIN7
23	GND	48	GND
24	FP_AIN2	49	FP_AIN4
25	FP_AIN1	50	FP_AIN3

Table 9-1 Multi-function I/O Connector (AgatePXC/2 Rev 1)

SDR Pin	Standard Pinout	SDR Pin	Standard Pinout	
1	MIPI_D3N	26	MIPI_D1N	
2	MIPI_CKN	27	MIPI_D0N	
3	MIPI_D3P	28	MIPI_D1P	
4	MIPI_CKP	29	MIPI_D0P	
5	GND	30	GND	
6	GND	31	GND	
7	MIPI_D2N	32	XMIP_SDA	
8	FP_HS_C_IN	33	FP_PWR	
9	MIPI_D2N	34	XMIP_SCL	
10	GND	35	GND	
11	GND	36	FP_R_IN	
12	FP_VS_IN	37	FP_G_IN	
13	FP_VS2	38	FP_B_IN	
14	FP_VIN4	39	FP_VIN8	
15	FP_VIN2	40	FP_VIN6	
16	GND	41	GND	
17	GND	42	GND	
18	FP_VIN3	43	FP_VIN7	
19	FP_VIN1	44	FP_VIN5	
20	FP_AIN4_CR2	45	FP_VIN8	Default = CR2
21	FP_AIN2	46	FP_AIN6_HS2	Default = HS2
22	GND	47	GND	
23	GND	48	GND	
24	FP_AIN3_MB2	49	FP_AIN7	Default = MB2
25	FP_AIN1	50	FP_AIN5_YG2	Default = YG2

9.2.2 CX3/FX3 SPI PROM Programming Application Note

9.2..2.1 Introduction

Due to an error in the design documentation from Cypress, the Agate Rev 1 CX3 and FX3 VUSB pins are connected to 3.3V instead of 5V, which is too low for the chips to recognize a valid VUSB. All standard FX3 and CX3 programs assume that VUSB is valid, and therefore will not work on Agate Rev 1. This includes the chips' internal USB autoboot program.

In order to make the Agate Rev 1 CX3 or FX3 operate, their associated SPI PROMs have to be loaded with a special Bootloader program that ignores VUSB.

All programs downloaded into Agate Rev 1 CX3 and FX3 SPI PROM must have a couple of extra lines of code inserted that make them ignore VUSB.

This loading had to be done using an EZ-USB FX3 Development Kit to initially program the CX3 and FX3 SPI PROMs with a Bootloader program that ignored VUSB. See the CYUSB3KIT-001 User Guide for more information about the Kit.

It is done by disabling the Kit's local SPI PROM. You then run jumpers from Kit J34 to the Agate CX3 SPI PROM or the FX3 SPI PROM.

Once the wiring is done, and with the Kit board set to USB Autoboot and the CX3 or FX3 held in reset, Cypress Control Center can communicate with the Kit and program the SPI PROM with the no-VUSB Bootloader. Of course, the SPI PROM being programmed is actually the CX3 or FX3 SPI PROM.

Needless to say, when testing new programs on the CX3 or FX3 for Agate Rev 1, **YOU MUST ALWAY RUN IN CX3 or FX3 SYSTEM MEMORY. DO NOT EVER USE SPI PROM** or it could render the CX3 or FX3 non-functional until the SPI wired kludge is redone and the Bootloader code is re-programmed in.

9.2..2.2 Modifying the DVK Board

It may be desired to make the EZ-USB FX3 Development Kit board emulate the usage Agate Rev 1 as much as possible in order to make things more realistic. One reason for doing this is to remove the VUSB so that if the program that is being tested doesn't have the VUSB patch, you can detect that before going to the trouble of putting in the Agate CX3 or FX3.

To that end, a few changes need to be made to the kit board. (See the schematics in this zip file for the references below):

a) Remove R62 (see schematic page 5) and wire its pads to the spare switch closure on SW25 (pins 4, 5) (see schematic page 2). Note that

(J102 2-3) must be installed. Putting this switch in allows the on board SPI PROM to be disabled.

1) If you want to use the on-board SPI PROM then this switch needs to be closed (in addition to other jumpers and switches being set - see below).

2) If you want to program off-board SPI PROMs, then this switch needs to be OFF.

Option (2) would be used for programming in no-VUSB Bootloader into the Agate Rev 1 CX3 or FX3. This when you have to run jumpers from J34 to the Agate CX3 SPI PROM or the FX3 SPI PROM pins.

All three Rev 1 Agates have already had the no-VBUS Bootloader programmed in so this option should not have to be used again unless you accidentally burn a program into the CX3 or FX3 that doesn't have the no-VUSB patch implemented.

Remember to always test a new program by using Option (1) above and testing to see if the Kit will still appear as a Bootloader in Control Center.

b) Remove U37 (see schematic page 9), which is a USB OVP. Using spare switch SW40-4 (see schematic page 6), wire U37-1 to SW40 pin 4 and U37-5 to SW40 pin 5.

This is done to see if test if the FX3 will work correctly with 5V VUSB but not 3.3V (and also if VUSB = 0) to make sure that the modified Bootloader and other programs really do have the no-VUSB patch correctly implemented:

By setting SW40-4 open, then VUSB = 0, which is effectively the same as 3.3V as the CX3 and FX3 won't work with VUSB < 4.0.

You can test a new program by setting SW40-4 open and programming the new program into local SPI PROM (Option 1 above).

In conclusion:

IF you are testing Agate Rev 1 programs,

1) you need to have SW40-4 OFF so that VUSB is off. Normal FX3 programs will not work with this switch off but programs built for the Agate should.

You want to make sure that Agate programs work in this mode - it's easier to debug than loading into the Agate and then the chip goes away. You usually have to reboot the whole board to recover.

2) you need to have the SW25-4 ON so that the FX3 will boot from the SPI PROM because the PROM has a no-VUSB bootloader programmed into it. The FX3 will not USB autoboot if SW40 4-5 is off.

3) you need to have the PMODE jumpers J96-J98 and SW25 set correctly to allow the SPI PROM to run:

SPI Boot - Agate Rev 1 testing

USB Boot - normal programs

	J98	**J97**	**J96**	**SW25-3**	**SW25-2**	**SW25-1**	**SW25-4**
SPI Boot (0F1)	2-3	none	2-3	ON	don't care	OFF	ON
USB Boot (F11)	none	2-3	2-3	don't care	OFF	OFF	don't care

For normal programs, it is still OK to boot from the SPI PROM, but you will need SW40-4 ON for them to run.

If you ever want to reprogram the local SPI PROM, you can do that by booting in USB mode and make sure that SW25-4 is ON

>>

We leave our in-house Kit board is set up to boot from SPI PROM but with SW40-4 ON so that normal programs will run.

To test Agate Rev 1 programs set SW40-4 OFF.

>>

Three other things -

The board does not need the power block that is included in the kit. It runs fine from a USB port. If you do want to use the power block, you have to change some jumpers.

It will go a lot faster if you have a USB 3.0 card, but works fine if you don't.

Note that the CX3 (or FX3) reset pin (C5) MUST BE DEASSERTED in order for the JTAG loop to work.

Chapter 10
Troubleshooting

10.1 General Procedures

The boards were designed with reliability and durability in mind. Nevertheless, it may happen that a problem will occur. This section is devoted to aiding the user in tracking down the problem efficiently and quickly.

You may be able to locate minor problems without technical assistance. If the problem cannot be remedied, Rastergraf can then issue a Return Material Authorization (RMA) so that the board can be returned to the factory for quick repair.

It can happen that installing a new board will overload the computer's power supply if the power supply margins are exceeded. The first step in ascertaining if this is the problem is to calculate a power supply budget. This involves adding up the power requirements of each board in the system to see if you are within specification. Consult your computer's technical manual for information on how to correctly determine this. A typical board will draw a total of less than 1A total at +5V and +3.3V.

When attempting to verify that the power supply is working properly, it is not unusual to unplug everything and measure the supply without a load. While this practice is acceptable for linear supplies, switching supplies (which are very commonly used in computers) require a certain load before proper regulation is achieved. Typically, at least 4A must be drawn from the +5V supply before all the other voltages are properly regulated.

It can also happen that if you build your own cables and you short F5V on the front panel connector to ground you may trigger the auto-resetting fuse which protects power supply pins when an overload occurs. The fuse resets automatically when an overload is removed.

Note

If the board is not functioning, check that +3.3V is supplied on the host side connectors. The boards **REQUIRE** both +3.3V and +5V. The boards can be supplied with a local +3.3V regulator, so if there is no way to supply +3.3V on the backplane, there is a way out. Please contact Rastergraf if you need to do this. In addition, -12V is required for Sync-On-Green (SOG) to work correctly.

10.2 Dealing with the PCI Bus

Because of the nature of the PCI protocol and the way support has been implemented in the Operating Systems for PCI bus devices such as the graphics board , it is not possible to follow the same debugging strategies.

In fact, there are no address jumpers for these boards. Everything is configured in software through a set of on-board registers, which control the characteristics of the board as required by the PCI Specification.

The information used to program these registers is supplied to Operating System (OS) specific functions by Rastergraf' software. Ordinarily, several address map translations occur, including the CPU physical and virtual address maps and the CPU to PCI bridge address map.

While x86 systems generally follow the standards required to meet PC compatibility and mask these details, PowerPC systems do not. Among PowerPC vendors, there are no standards which ensure interoperability among CPU boards, even when they use the same CPU and PCI bridge.

Therefore, if you plan to use a graphics board in a PowerPC based system, it is vital to ensure that Rastergraf can vouch for the board's operation before you order the board. Otherwise, you may go crazy trying to figure out why it doesn't work. Please contact us (support@rastergraf.com or at (541) 923-5530 if you have problems.

10.3 Maintenance, Warranty, and Service

10.3.1 Maintenance

The graphics board requires no regular service, but if used in a particularly dirty environment, periodic cleaning with dry compressed air is recommended.

Because of the heat generated by normal operation of the graphics board and other boards in the system, forced cross flow ventilation ***is required***. If forced ventilation is not used, IC temperatures can rise to 60 degrees C or higher, which can cause premature product failure. With proper forced air-cooling IC temperatures will be less than 35 degrees C.

10.3.2 Warranty

The graphics boards are warranted to be free from defects in material or manufacture for a period of 12 months from date of shipment from the factory. Rastergraf' obligation under this warranty is limited to replacing or repairing (at its option) any board which is returned to the factory within this warranty period and is found by Rastergraf to be defective in proper usage. This warranty does not apply to modules which have been subjected to mechanical and/or electrical abuse, overheating, or other improper usage. This warranty is made in lieu of all other warranties expressed or implied. **All warranty repair work will be done at the Rastergraf factory.**

10.3.3 Return Policy

Before returning a module the customer must first request a Return Material Authorization (RMA) number from the factory. The RMA number must be enclosed with the module when it is packed for shipment. A written description of the trouble should also be included.

Customer should prepay shipping charges to the factory. Rastergraf will prepay return shipping charges to the customer. Repair work is normally done within ten working days from receipt of module.

10.3.4 Out of Warranty Service

Factory service is available for modules which are out of warranty or which have sustained damage making them ineligible for warranty repair. A flat fee will be charged for normal repairs and must be covered by a valid purchase order. If extensive repairs are required, Rastergraf will request authorization for an estimated time and materials charge. If replacement is required, additional authorization will be requested.

All repair work will be done at the Rastergraf factory in Redmond, Oregon, unless otherwise designated by Rastergraf.

Index